High-Efficiency Ultracapacitor Charger Using a Soft-Switching Full-Bridge DC-DC Converter

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Abstract—This paper proposes a high-efficiency ultracapacitor charger using a soft-switching full-bridge pulse-width modulated (PWM) converter. Conventional full-bridge phase-shift modulated (PSM) converter is used for charging ultracapacitors. However, the power efficiency of conventional converters is low because of its circulating current and high output diode voltage stresses. This study presents a high-efficiency full-bridge PWM converter to overcome the drawbacks of conventional converters. The proposed converter has the advantages of lower switch voltage stresses and reduced circulating current compared to other converter topologies. The performance of the proposed converter is evaluated by experimental results for a 54-V, 35-F ultracapacitor bank.

I. INTRODUCTION

Ultracapacitors have been widely used for electric vehicle chargers and energy conversion systems because of their high power density [1]. Its reliability and stability depend on several factors such as charge mode, age, temperature, and maintenance [2]. Ultracapacitors are charged with a certain current and voltage levels by an ultracapacitor charger [3]. The basic requirements for ultracapacitor chargers are small size and high efficiency. A high switching frequency is necessary to achieve a small size. However, as the switching frequency is increased, the power efficiency of the ultracapacitor chargers is reduced because of increased switching losses [4]. Thus, selecting an optimal converter topology is important for the design of high-efficiency ultracapacitor chargers.

The full-bridge phase-shift modulated (PSM) converter is a popular DC-DC converter for low-voltage and high-current charging applications [5]-[12]. Particularly, the full-bridge PSM converter with a current-doubler rectifier (CDR) in Fig. 1 is a good candidate for ultracapacitor chargers due to its high power capability and soft-switching operation [7]-[9]. Power switches operate at zero-voltage switching (ZVS) conditions, reducing switching power losses. However, the conventional full-bridge PSM converter with a CDR has several drawbacks such as high circulating currents and high output diode voltage stresses. Because of the phase-shifted switching operation between two switching legs, high circulating current flows at the primary side, causing high conduction losses [7], [8]. In addition, at the secondary side, the output diodes suffer from high voltage stresses because of the high voltage spikes at their turn-off instance [7], [9]. These drawbacks results in decreased power efficiency and causes additional thermal management problems.

In order to alleviate the above-mentioned problems, a high-efficiency full-bridge converter with a CDR is proposed for charging ultracapacitors. The proposed converter in Fig. 2 can reduce circulating currents and output diode voltage stresses by applying a constant frequency pulse-width modulation (PWM)
II. PROPOSED CONVERTER

Fig. 2 shows a circuit diagram of the proposed converter. $V_{in}$ is the input voltage. $V_o$ is the output voltage. The primary part circuit consists of power switches ($S_1, S_2, S_3, S_4$), a clamping capacitor ($C_c$), and a transformer ($T$). The full-bridge switching circuit consists of $S_1, S_2, S_3, S_4$, and $C_c$ at the primary side. The power switches are considered ideal switches except body diodes $D_1 \sim D_4$ and output capacitors $C_1 \sim C_2$. The transformer $T$ has a magnetizing inductor $L_m$ and leakage inductor $L_{lk}$ with the turns ratio of $1 : N$ where $N = N_p/N_p'$. The secondary part circuit consists of output diodes ($D_{o1}, D_{o2}$), and output inductors ($L_2, L_3$). The CDR consists of $D_{o1}, D_{o2}, L_1,$ and $L_2$ at the secondary side.

Fig. 3 shows the operation modes of the proposed converter during one switching period $T_s$. The converter has four switching modes during $T_s$. Fig. 4 shows the switching waveforms of the proposed converter during $T_s$. $S_1$ ($S_3$) and $S_2$ ($S_4$) are turned on and off simultaneously. Then, $S_1$ ($S_3$) and $S_2$ ($S_4$) operate complementarily with a short dead time. The duty ratio $D$ is based on the on-time of $S_1$ and $S_2$. Then, the duty ratio of $S_1$ and $S_2$ is $1 - D$. Before $t = t_{on}$, $S_1$ and $S_2$ have been turned off. The voltages $V_{s1}$ and $V_{s2}$ have been zero when the primary current $i_p$ flows through body diodes $D_1$ and $D_2$.

Mode 1 [$t_{on}, t_1$]: At $t = t_{on}$, $S_1$ and $S_2$ are turned on at zero-voltage. Since $L_m$ and $L_0$ store energy from $V_{on}$, the magnetizing inductor current $i_{lm}$ increases linearly as:

$$i_{lm}(t) = i_{lm}(t_0) + \frac{V_{on}}{L_m + L_{lk}}(t - t_0).$$

At the secondary side, output diode $D_{o1}$ is turned on. The output inductor current flows through diode $D_{o1}$.

Mode 2 [$t_1, t_2$]: At $t = t_1$, $S_1$ and $S_2$ are turned off. The primary current $i_p$ charges $C_1$ and $C_2$, and discharges $C_3$ and $C_4$. $V_{s1}$ increases from zero to $V_{in}$, while $V_{s2}$ increases from zero to $V_{in} + V_t$. $V_{s3}$ decreases from $V_{in} + V_t$ to zero while $V_{s4}$ decreases from $V_{in}$ to zero. Since the switch output capacitor $C_o$ ($= C_1 = C_2 = C_3 = C_4$) is very small, the time interval during this mode is considered negligible when compared to $T_s$. The magnetizing current $i_{lm}$ is considered to be constant. Switch body diodes $D_1$ and $D_2$ conduct the primary current $i_p$ at the end of this mode.

Mode 3 [$t_2, t_3$]: At $t = t_2$, $S_1$ and $S_2$ are turned on at zero-voltage. The energy stored in $L_m$ and $L_0$ is recycled to the clamping capacitor $C_c$. Then, $S_1$ and $S_2$ are turned on without...
primary current output inductor current flows through diode. The magnetizing inductor current and decreases linearly as:

\[ i_{Lm}(t) = i_{Lm}(t_2) - \frac{(V_{in} + V_c)}{L_m + L_{in}}(t - t_2). \] (2)

At the secondary side, output diode \( D_{o2} \) is turned on. The output inductor current flows through diode \( D_{o2} \).

Mode 4 \([t_3, t_4]\): At \( t = t_3 \), 31 and 32 are turned off. The primary current \( i_p \) charges \( C_3 \) and \( C_4 \) and discharges \( C_3 \) and \( C_4 \). \( V_{s3} \) decreases from \( V_{in} \) to zero while \( V_{s4} \) decreases from \( V_{in} + V_c \) to zero. \( V_{s3} \) increases from zero to \( V_{in} + V_c \) while \( V_{s4} \) increases from zero to \( V_{in} \). Switch body diodes \( D_1 \) and \( D_2 \) conduct the primary current \( i_p \). The next switching cycle begins when \( S_1 \) and \( S_2 \) are turned on at zero-voltage again. For the volt-second balance relation on \( L_m \) during \( t_m \), the voltage \( V_c \) is expressed as:

\[ V_c = \frac{2D - 1}{1 - D} V_{in}. \] (3)

For the volt-second balance relation on \( L_1 \) and \( L_2 \) during \( T_m \), the following relation between \( V_{in} \) and \( V_o \) is obtained as:

\[ \frac{V_o}{V_{in}} = ND. \] (4)

In the proposed converter, the voltage stress of \( S_1 \) and \( S_2 \) is clamped to the input voltage. On the other hand, the voltage stress of \( S_2 \) and \( S_3 \) is the sum of the input voltage and the clamping capacitor voltage. The voltage stress of \( S_2 \) and \( S_3 \) can be changed with the duty ratio \( D \). When the duty ratio \( D \) is below 0.5, the voltage stress of \( S_1 \) and \( S_2 \) can be lower than the input voltage \( V_{in} \). It is one of the advantages of the proposed converter when compared to the conventional full-bridge PSM converter. The conventional full-bridge PSM converter has a circulating current during freewheeling period. The circulating current causes the conduction losses. The power is not delivered to the secondary side even though the current is circulating at the primary side. However, the proposed converter is no freewheeling period except for a small dead time period. As a result, the proposed converter can be minimized circulating current. Thus, conduction losses are reduced significantly. This is another advantage of the proposed converter when compared to the conventional full-bridge PSM converter.

III. CONTROL STRATEGY

Fig. 5 shows a control block diagram of the proposed converter based on a constant current and constant voltage control [13]. It is assumed that the output inductor current \( i_L \) flows continuously. Two control loops are used: an inner current control loop and an outer voltage control loop. The duty ratio \( D \) is expressed as:

\[ D = D_n + D_c \] (5)

\( D_n \) is a nominal duty ratio. \( D_c \) is a controlled duty ratio. \( D_n \) and \( D_c \) can be represented respectively as:

\[ D_n = \frac{V_o}{NV_m} \] (6)

\[ D_c = k_p i_{err} + k_i \int i_{err} dt \] (7)

where \( i_{err} = i_L^{*} - i_L \). The current error \( i_{err} \) is calculated by comparing the current command \( i_L^{*} \) to the measured battery current \( i_L \). \( k_p \) and \( k_i \) are the proportional and integral control gains, respectively. To regulate the battery voltage \( V_o \) a PI-type voltage controller is used. The voltage error \( V_{err} \) is calculated by comparing the reference battery voltage \( V_o^{*} \) to the

\[ V_o^{*} + \sum V_{corr} \rightarrow \text{Voltage controller} \rightarrow i_L^{*} \rightarrow \text{Current limiter} \rightarrow \sum k_{err} \rightarrow \text{Current controller} \rightarrow \sum D \rightarrow V_o \rightarrow \frac{V_o}{NV_m} \]

Fig. 5. Control block diagram of the proposed converter.

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measured battery voltage $V_o$. The voltage controller generates the current command $i_L^*$ which is the maximum charging current of the battery. If $i_L^*$ is higher than $i_{L\text{ limit}}$, the battery is charged with a constant current. By contrast, if $i_L^*$ is lower than $i_{L\text{ limit}}$, the battery is charged with a constant voltage. The addition of the open loop duty ratio $D_n$ relaxes the burden of the current controller, improving the dynamic response of the controlled system.

The controller is digitally implemented by using a single-chip microcontroller dsPIC30F3011 (Mircochip). The microcontroller provides a function of 16-bit fixed-point arithmetic, including a significant support for DSP. It has various peripherals directed toward a single-chip solution for digital control of power electronic converters. The program structure can be divided into initialization, control, and PWM generation. At the beginning of the main program, the system registers and control parameters are initialized. The control routine is activated every 100 μsec period by the timer interrupt. The input voltage $V_d$, battery voltage $V_b$, and battery current $i_b$ are measured by the voltage and current sensing amplifiers. They are sensed through the 10-bit A/D converter in the microcontroller. After the voltage and current signals are read, the duty ratio $D$ is obtained by calculating $D_n$ and $D_c$. The power supply PWM module in the dsPIC30F3011 generates the complementary duty signals for power switches.
A 1.0 kW prototype circuit has been designed and tested to verify the operation principles and performance of the proposed converter. The input voltage ranges from 350 V to 400 V. An ultracapacitor bank is used, which consists of 20 ultracapacitors connected in series. The rated capacitance per capacitor is 700 F. Its rated voltage is 2.7 V. Its equivalent resistance is 4.5 mΩ. The total equivalent capacitance of the ultracapacitor bank is 90 mF. The total equivalent capacitance of the ultracapacitor bank is 35 F. The output voltage of the converter ranges from 30 V to 48 V, considering the rated voltage of the ultracapacitor bank. The power switches $S_1 = S_2 = FQA24N60NF$ (Fairchild) and power diodes are $D_{s1} = D_{s2} = F15U40S$ (Fairchild) are used. The power switches operate at a constant switching frequency of 60 kHz with a dead time 330 nsec. The transformer $T$ has a primary winding turns of $N_p = 35$ and a secondary winding turns of $N_s = 12$.

The conventional full-bridge PSM converter has been designed and tested for a performance comparison with the proposed converter. Fig. 6 shows the experimental waveforms of the conventional full-bridge PSM converter. Fig. 6(a) shows the primary current $i_p$ and switch voltages $V_{s1}$ and $V_{s2}$. Fig. 6(b) shows the output inductor current $i_o$ and output diode voltages $V_{d12}$ and $V_{d21}$. It is observed that the circulating current flows at the primary side, which causes high conduction losses.

Fig. 7 shows the experimental waveforms of the proposed converter when the duty ratio $D$ is 0.4. Fig. 7(a) shows the primary current $i_p$ and switch voltages $V_{s1}$ and $V_{s2}$. Fig. 7(b) shows the primary current $i_p$ and switch voltages $V_{s2}$ and $V_{s3}$. Fig. 7(c) shows the output inductor current $i_o$ and output diode voltages $V_{d12}$ and $V_{d21}$. ZVS of the power switches is achieved, which significantly reduces the switching power losses. The output diode voltage stresses of the proposed converter in Fig. 7(c) are reduced compared to the output diode voltage stresses of the conventional full-bridge PSM converter in Fig. 6(b).

Fig. 8 shows the measured efficiencies of the converters for different output load conditions. The conventional full-bridge PSM converter achieves an efficiency of 93.0% at 350 V input voltage and 48 V output voltage for an 1.0 kW output power. On the other hand, the proposed converter achieves a high-efficiency of 94.0% at 350 V input voltage and 48 V output voltage for an 1.0 kW output power. The proposed converter improves the power efficiency by 1.0% by minimizing the conduction losses and by reducing switching losses.

V. CONCLUSIONS

This paper proposed a high-efficiency ultracapacitor charger using a soft-switching full-bridge PWM converter. The proposed converter provides wide ZVS range of power switches. Circulating currents are decreased without the freewheeling period. Switching losses can be reduced by extending ZVS range. Conduction losses are minimized by eliminating circulating current. A constant current and constant voltage charging is performed. Experimental results are provided to verify the operation of the proposed converter. The performance of the proposed converter has been evaluated by experiments for charging a 35 F ultracapacitor bank. The proposed converter achieves a high efficiency of 94.0% for a 1.0 kW output power. It achieves a higher efficiency compared to the conventional full-bridge converter with a PSM.

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