ADVANCED MULTI-QUADRANT OPERATION
DC/DC CONVERTERS

Fang Lin Luo
Hong Ye

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Preface

DC/DC converters are systematically sorted into 6 generations. We introduce the DC/DC converters of the second to fourth generations in this book. The purpose of this book is to provide multi-quadrant operation DC/DC converters that are both concise and useful for engineering students and practicing professionals. It is well organized in 200 pages and 100 diagrams to introduce more than 50 topologies of the multi-quadrant DC/DC converters. All topologies are novel approaches and new contributions to modern power electronics. They are sorted into three generations:

1. Second generation (multiple-quadrant) converters
2. Third generation (switched component) converters
3. Fourth generation (soft-switching) converters

The second generation (multiple-quadrant) converters have a large number of prototypes published in the literature. We introduce the multiple quadrant operation Luo-converters in this book to summarize this technique. From these examples, people can understand the basics of designing a multiple-quadrant converter.

The third generation (switched component) converters involve switched capacitor (SC) converters and switched inductor (SI) converters. Since switched capacitors can be integrated into a power integrated circuit (IC) chip, SC converters are small and have a high power density. However, most of the published papers avoid discussing the efficiency because most SC converters possess low power transfer efficiency. A two-quadrant SC DC/DC converter implementing voltage lift and current amplification techniques with high efficiency, high power density, and low electromagnetic interference (EMI) is introduced in this book.

SC converters can perform four-quadrant operations. Since they are required for communication equipment and industrial applications, we carefully discuss these converters.

SC converters are always performing in push-pull state, and control circuitry is complex. A large number of capacitors are required, especially in the case of large differences between input and output voltages. SI DC/DC converters are a different prototype of DC/DC conversion technology from SC converters. SI DC/DC converters’ advantages include simple structure, simple control circuitry, high efficiency, large power and high-power density. Usually, one inductor is required for a SI DC/DC converter. Since it consists of only one inductor, its size is small. This type of converter has outstanding advantages: no matter how many quadrant operations or how large the
difference between input and output voltages, only one inductor is usually employed in one SI DC/DC converter.

The fourth generation (soft-switching) converters involve the following types:

- Zero-current-switching (ZCS) converters
- Zero-voltage-switching (ZVS) converters
- Zero-transition (ZT) converters

A large number of the soft-switching converters have been published in the literature since the 1980s. Most papers introduce signal-quadrant operation soft-switching converters. We introduced our work on multi-quadrant operation soft-switching converters in this book.

This book is organized into five chapters. The multiple-quadrant operating Luo-converters are introduced in Chapter 1; and switched component (SC and SI) converters in Chapter 2. Chapters 3 and 4 introduce the multiple-lift push-pull switched-capacitor converters. Chapter 5 introduces the multiple-quadrant soft-switch converters.

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Classical DC-DC converters usually perform in single quadrant operation, such as buck converters and Luo-converters. Multiple-quadrant operation is required in industrial applications, e.g., a DC motor running forward and reverse in motoring and regenerative braking states. This chapter introduces three new converters that can perform two- and four-quadrant DC/DC conversion. One particular application is the MIT 42/±14 V DC/DC converter used for new car power supply systems. Because this converter implements dual-direction energy transference, it is a second-generation DC/DC converter. Simulation and experimental results have verified its characteristics.

1.1 Introduction

Multiple-quadrant operation converters can be derived from the multiple-quadrant chopper. Correspondingly, class B converters can be derived from type B choppers (two-quadrant operation), class E converters from type E choppers (four-quadrant operation) and so on. Also, multiple-quadrant operation converters can be derived from other first generation converters. This chapter introduces two- and four-quadrant operation Luo-converters, which are derived from positive, negative and double output Luo-converters. They correspond to a DC motor drive in forward and reverse running with motoring and regenerative braking states. These converters are shown in Figure 1.1. The input source and output load are usually certain voltages as shown $V_1$ and $V_2$. Switches $S_1$ and $S_2$ in this diagram are power MOSFET devices, and driven by a pulse-width-modulated (PWM) switching signal with repeating frequency $f$ and conduction duty $k$. In this chapter the switch repeating period is $T = 1/f$, the switch-on period is $kT$ and switch-off period is $(1 - k)T$. The equivalent resistance is $R$ for each inductor. During switch-on the voltage drop across the switches and diodes are $V_S$ and $V_D$. When the switch is turned off, the free-wheeling diode current descends in whole switch-off period $(1 - k)T$. If the diode current does not become zero before
the switch is turned on again, we define this working state to be the continuous region. If the current becomes zero before the switch is turned on again, this working state is the discontinuous conduction region.

In this chapter, variation ratio of current $i_{L1}$ is

$$\xi_{L1} = \frac{\Delta i_{L1}}{2 I_{L1}}$$
Variation ratio of current $i_{L2}$ is

$$\xi_{L2} = \frac{\Delta i_{L2}}{I_{L2}}$$

Variation ratio of current $i_D$ is

$$\zeta = \frac{\Delta i_D}{I_D}$$

Variation ratio of voltage $v_C$ is

$$\rho = \frac{\Delta v_C}{V_C}$$

1.2 Circuit Explanation

Each converter shown in Figure 1.1 consists of two switches with two passive diodes, two inductors and one capacitor. Circuit 1 performs a two-quadrant (forward) operation, and circuit 2 performs a two-quadrant (reverse) operation. Circuit 1 and circuit 2 can be converted to each other by a three-pole (A, B, and C) double-through (A1/A2, B1/B2, and C1/C2) auxiliary changeover switch as circuit 3. Circuit 3 performs a four-quadrant operation. Since the change-over process between forward and reverse operations is not very frequent, so that the auxiliary change-over switch can be isolated-gate bipolar transistor (IGBT), power relay and contactor. The source voltage ($V_1$) and load voltage ($V_2$) are usually considered as constant voltages. The load can be a battery or motor back electromotive force (EMF). For example, when the source voltage is 42 V and load voltage is ±14 V there are four modes of operation:

1. Mode A (Quadrant I): electrical energy is transferred from source side $V_1$ to load side $V_2$
2. Mode B (Quadrant II): electrical energy is transferred from load side $V_2$ to source side $V_1$
3. Mode C (Quadrant III): electrical energy is transferred from source side $V_1$ to load side $-V_2$
4. Mode D (Quadrant IV): electrical energy is transferred from load side $-V_2$ to source side $V_1$

Each mode has two states: on and off. Circuit 1 in Figure 1.1a implements Modes A and B, and Circuit 2 in Figure 1.1b implements Modes C and D.
1.2.1 Mode A

Mode A implements the characteristics of the buck-boost conversion. For mode A, state-on is shown in Figure 1.2a: switch $S_1$ is closed, switch $S_2$ and diodes $D_1$ and $D_2$ are not conducted. In this case inductor currents $i_{L1}$ and $i_{L2}$ increase, and $i_1 = i_{L1} + i_{L2}$. State-off is shown in Figure 1.2b: switches $S_1$, $S_2$, and diode $D_1$ are off and diode $D_2$ is conducted. In this case current $i_{L1}$
flows via diode $D_2$ to charge capacitor $C$, in the meantime current $i_{L2}$ is kept to flow through load battery $V_2$. The free-wheeling diode current $i_{D2} = i_{L1} + i_{L2}$. Some currents' and voltages' waveforms are shown in Figure 1.2c.

1.2.2 Mode B

Mode B implements the characteristics of the boost conversion. For mode B, state-on is shown in Figure 1.3a: switch $S_2$ is closed, switch $S_1$ and diodes $D_1$ and $D_2$ are not conducted. In this case inductor current $i_{L2}$ increases by biased...
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$V_2$, inductor current $i_{L1}$ increases by biased $V_C$. Therefore capacitor voltage $V_C$ reduces. State-off is shown in Figure 1.3b: switches $S_1$, $S_2$ and diode $D_2$ are not on, and only diode $D_1$ is on. In this case source current $i_1 = i_{L1} + i_{L2}$ which is a negative value to perform the regenerative operation. Inductor current $i_{L2}$ flows through capacitor $C$, it is charged by current $i_{L2}$. After capacitor $C$, $i_{L2}$ then flows through the source $V_1$. Inductor current $i_{L1}$ flows through the source $V_1$ via diode $D_1$. Some currents’ and voltages’ waveforms are shown in Figure 1.3c.

1.2.3 Mode C

Mode C implements the characteristics of the buck-boost conversion. For mode C, state-on is shown in Figure 1.4a: switch $S_1$ is closed, switch $S_2$ and diodes $D_1$ and $D_2$ are not conducted. In this case inductor currents $i_{L1}$ and $i_{L2}$ increase, and $i_1 = i_{L1}$. State-off is shown in Figure 1.4b: switches $S_1$, $S_2$ and diode $D_1$ are off and diode $D_2$ is conducted. In this case current $i_{L1}$ flows via diode $D_2$ to charge capacitor $C$ and the load battery $V_2$ via inductor $L_2$. The free-wheeling diode current $i_{D2} = i_{L2}$ flows through capacitor $C$ that is charged by current $i_{L2}$, i.e., $i_{D2} = i_{L2}$. Some waveforms are shown in Figure 1.4c.

1.2.4 Mode D

Mode D implements the characteristics of the boost conversion. For mode D, state-on is shown in Figure 1.5a: switch $S_2$ is closed, switch $S_1$ and diodes $D_1$ and $D_2$ are not conducted. In this case inductor current $i_{L1}$ increases by biased $V_2$, inductor current $i_{L2}$ decreases by biased $(V_2 - V_C)$. Therefore capacitor voltage $V_C$ reduces. Current $i_{L1} = i_{C-off} + i_2$. State-off is shown in Figure 1.5b: switches $S_1$, $S_2$ and diode $D_2$ are not on, and only diode $D_1$ is on. In this case source current $i_1 = i_{L1}$ which is a negative value to perform the regenerative operation. Inductor current $i_{L2}$ flows through capacitor $C$ that is charged by current $i_{L2}$, i.e., $i_{L2} = i_2$. Some currents and voltages waveforms are shown in Figure 1.5c.

1.2.5 Summary

The switch status of all modes is listed in Table 1.1. From the table it can be seen that only one switch works in on mode, so that this converter is very simple and effective.

1.3 Mode A (Quadrant I Operation)

As shown in Figure 1.2a and b the voltage across capacitor $C$ increases during switch-on, and decreases during switch-off. Capacitor $C$ acts as the primary
means of storing and transferring energy from the input source to the output load via the pump inductor $L_1$. Assuming capacitor $C$ to be sufficiently large, the variation of the voltage across capacitor $C$ from its average value $V_C$ can be neglected in steady state, i.e., $v_c(t) = V_C$, even though it stores and transfers energy from the input to the output.

### 1.3.1 Circuit Description

When switch $S_1$ is on, the source current $i_s = i_{L1} + i_{L2}$. Inductor $L_1$ absorbs energy from the source. In the mean time inductor $L_2$ absorbs energy from the output.
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FIGURE 1.5
Mode D.

TABLE 1.1
Switch Status

<table>
<thead>
<tr>
<th>Switch or Diode</th>
<th>Circuit</th>
<th>Mode A (QI)</th>
<th>Mode B (QII)</th>
<th>Mode C (QIII)</th>
<th>Mode D (QIV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>State-on</td>
<td>State-off</td>
<td>State-on</td>
<td>State-off</td>
</tr>
<tr>
<td>S₁</td>
<td>Circuit 1</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>D₁</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>S₂</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>D₂</td>
<td>ON</td>
<td>ON</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: The blank status means OFF.
source and capacitor C, both currents $i_{L1}$ and $i_{L2}$ increase. When switch $S_1$ is off, source current $i_s = 0$. Current $i_{L1}$ flows through the free-wheeling diode $D_2$ to charge capacitor C. Inductor $L_1$ transfers its stored energy to capacitor C. In the mean time current $i_{L2}$ flows through the load $V_2$ and free-wheeling diode $D_2$ to keep itself continuous. Both currents $i_{L1}$ and $i_{L2}$ decrease. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 1.2c. The equivalent circuits in switch-on and -off states are shown in Figure 1.2a and b.

Actually, the variations of currents $i_{L1}$ and $i_{L2}$ are small so that

$$i_{L1} = I_{L1} \quad \text{and} \quad i_{L2} = I_{L2}$$

The charge on capacitor C increases during switch off and on:

$$Q^+ = (1 - k)T_i \quad I_{L1}$$

$$Q^- = kT I_{L2}$$

In a whole period investigation, $Q^+ = Q^-$. Thus,

$$I_{L2} = \frac{1-k}{k} I_{L1} \quad (1.1)$$

Since capacitor C performs as a low-pass filter, the output current

$$I_{L2} = I_2$$

The source current $i_s = i_{L1} + i_{L2}$ during switch-on, and $i_s = 0$ during switch-off. Average source current $I_s$ is

$$I_s = k \times i_s = k(i_{L1} + i_{L2}) = k(1 + \frac{1-k}{k}) I_{L1} = I_{L1}$$

Hence, the output current is

$$I_2 = \frac{1-k}{k} I_1 \quad (1.2)$$

The input and output powers are

$$P_i = V_i I_1 \quad \text{and} \quad P_o = V_o I_2$$

The power losses are
$V_s l_1$ — Switch power loss
$R l_1^2$ — Power loss across inductor $L_1$
$V_d I_1$ — Diode power loss
$R l_2^2$ — Power loss across inductor $L_2$

The total power losses are

$$P_{\text{loss}} = V_s I_1 + V_d I_1 + R(I_1^2 + I_2^2)$$

(1.3)

Since

$$P_l = P_o + P_{\text{loss}}$$

hence

$$V_s I_1 = V_2 I_2 + (V_s + V_d) I_1 + R(I_1^2 + I_2^2)$$

(1.4)

or

$$V_s = V_2 \left( \frac{1-k}{k} \right) + (V_s + V_d) + R I_2 \left( \frac{k}{1-k} + \frac{1-k}{k} \right)$$

(1.5)

The output current is

$$I_2 = \frac{V_s - V_d - V_2(1-k)}{R \left( \frac{k}{1-k} + \frac{1-k}{k} \right)}$$

(1.6)

The minimum conduction duty $k$ corresponding to $I_2 = 0$ is

$$k_{\text{min}} = \frac{V_2}{V_1 + V_2 - V_s - V_d}$$

(1.7)

The power transfer efficiency is

$$\eta_A = \frac{P_o}{P_l} = \frac{V_s I_2}{V_1 I_1} = \frac{1}{1 + \frac{V_s + V_d}{V_2} \cdot \frac{k}{1-k} + \frac{R I_2}{V_2} \left[ 1 + \left( \frac{1-k}{k} \right)^2 \right]}$$

(1.8)
1.3.2 Variations of Currents and Voltages

Because the voltage across the inductor $L_1$ is $(V_1 - RI_1)$ during switch-on and $(V_C + RI_1)$ during switch-off, the average voltage across capacitor $C$ is

$$kT(V_1 - RI_1) = (V_C + RI_1)(1-k)T$$

Hence

$$V_C = \frac{k}{1-k}V_1 - \frac{1}{1-k}RI_1 = \frac{k}{1-k}V_1 - RI_2 = \frac{k}{1-k}(V_1 - \frac{RI_2}{1-k})$$ (1.9)

The peak-to-peak variation of capacitor voltage $v_C$ is

$$\Delta v_C = \frac{Q_j}{C} = \frac{kT I_2}{C} = k \frac{I_2}{fC}$$

The variation ratio of capacitor voltage $v_C$ is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{(1-k)I_2}{2fC(V_1 - RI_1 \frac{1}{1-k})}$$ (1.10)

The peak-to-peak variation of inductor current $i_{L1}$ is

$$\Delta i_{L1} = \frac{V_1 - V_S - RI_1}{L_1} kT$$

The variation ratio of inductor current $i_{L1}$ is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = k \frac{V_1 - V_S - RI_1}{2fL_1 I_1}$$ (1.11)

The peak-to-peak variation of inductor current $i_{L2}$ is

$$\Delta i_{L2} = \frac{V_1 - V_S - V_C + V_C - RI_2}{L_2} kT = \frac{V_1 - V_S - RI_1}{L_2} kT$$

The variation ratio of inductor current $i_{L2}$ is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = k \frac{V_1 - V_S - RI_1}{2fL_2 I_2}$$ (1.12)
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The free-wheeling diode’s current \( i_{D2} \) during switch off is: \( i_{D2} = i_{L1} + i_{L2} \). Its peak-to-peak variation is

\[
\Delta i_{D2} = \Delta i_{L1} + \Delta i_{L2} = \frac{V_1 - V_2 - RI_1}{L} kT
\]

where

\[
L = \frac{L_1 L_2}{(L_1 + L_2)}.
\]

The variation ratio of the diode current \( i_{D2} \) is

\[
\zeta_{D2} = \frac{\Delta i_{D2}}{I_{L1} + I_{L2}} = k \frac{V_1 - V_2 - RI_1}{2fL(I_1 + I_2)} = k^2 \frac{V_1 - V_2 - RI_1}{2fLI_1}
\]

(1.13)

1.3.3 Discontinuous Region

If the diode current becomes zero before \( S_1 \) switch is on again, the converter works in discontinuous region. The condition \( i_{D2} \zeta_{D2} = 1 \), i.e.,

\[
k^2 = \frac{2fLI_1}{V_1 - V_2 - RI_1}
\]

(1.14)

From Equations (1.7) and (1.14) the boundary between continuous and discontinuous regions is shown in Figure 1.6. Particularly, since conduction duty \( k \) is greater than \( k_{\text{min}} \) and the current is high, the converter usually works in the continuous region.
1.4 Mode B (Quadrant II Operation)

As shown in Figure 1.3a and b the voltage across capacitor $C$ decreases during switch-on, and increases during switch off. Capacitor $C$ acts as the primary means of storing and transferring energy from the load battery to the source via inductor $L_2$. Assuming capacitor $C$ to be sufficiently large, the variation of the voltage across capacitor $C$ from its average value $V_C$ can be neglected in steady state, i.e., $v_C(t) = V_C$, even though it stores and transfers energy from the load $V_2$ to the source $V_1$.

1.4.1 Circuit Description

When switch $S_2$ is off, source current $i_1 = 0$. Current $i_{L1}$ flows through the switch $S_2$ and capacitor $C$, and increases. Current $i_{L1}$ flows through the switch $S_2$, and increases. When switch $S_2$ is off, the source current $i_1 = i_{L1} + i_{L2}$. The free-wheeling diode $D_1$ is conducted. Both currents $i_{L1}$ and $i_{L2}$ decrease. Inductor $L_1$ transfers its stored energy to capacitor $C$. In the mean time current $i_{L2}$ flows through the source $V_1$. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 1.3c. The equivalent circuits in switch-on and -off states are shown in Figures 1.3a and b.

Actually, the variations of currents $i_{L1}$ and $i_{L2}$ are small so that $i_{L1} = I_{L1}$ and $i_{L2} = I_{L2}$

The charge on capacitor $C$ increases during switch off and on:

$Q^+ = (1 - k)T \cdot I_{L2}$

$Q^- = kT \cdot I_{L1}$

In a whole period investigation, $Q^+ = Q^-$. Thus,

$I_{L1} = \frac{1 - k}{k} \cdot I_{L2}$  \hspace{1cm} (1.15)

Since capacitor $C$ performs as a low-pass filter, the output current

$I_{L2} = I_2$

The source current $i_1 = i_{L1} + i_{L2}$ during switch-on, and $i_1 = 0$ during switch-off. Average source current $I_1$ is

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\[ I_1 = (1 - k)i_1 = (1 - k)(i_{L1} + i_{L2}) = (1 - k)(1 + \frac{1}{1 - k})I_{L1} = I_{L1} \]

Hence, the output current is

\[ I_1 = \frac{1 - k}{k} I_2 \quad (1.16) \]

The input and output powers are

\[ P_i = V_2 I_2 \quad \text{and} \quad P_o = V_1 I_1 \]

The power losses are

- \( V_S I_1 \) — Switch power loss
- \( RL_{L1}^2 \) — Power loss across inductor \( L_1 \)
- \( V_D I_1 \) — Diode power loss
- \( RL_{L2}^2 \) — Power loss across inductor \( L_2 \)

The total power losses are

\[ P_{loss} = V_S I_1 + V_D I_1 + R(I_1^2 + I_2^2) \quad (1.17) \]

Since

\[ P_i = P_o + P_{loss} \]

hence

\[ V_2 I_2 = V_1 I_1 + (V_S + V_D) I_1 + R(I_1^2 + I_2^2) \quad (1.18) \]

or

\[ V_2 = \frac{1 - k}{k} (V_1 + V_S + V_D) + R I_1 (\frac{k}{1 - k} + \frac{1 - k}{k}) \quad (1.19) \]

The output current is

\[ I_1 = \frac{V_2 - (V_1 + V_S + V_D) \frac{1 - k}{k}}{R(\frac{k}{1 - k} + \frac{1 - k}{k})} \quad (1.20) \]
The minimum conduction duty $k$ corresponding to $I_1 = 0$ is

$$k_{\text{min}} = \frac{V_1 + V_S + V_D}{V_1 + V_2 + V_S + V_D}$$  \hfill (1.21)

The power transfer efficiency is

$$\eta_B = \frac{P_O}{P_I} = \frac{V_{11}}{V_{22}} = \frac{1}{1 + \frac{V_S + V_D}{V_1} + \frac{RI_1}{V_1} \left[1 + \left(\frac{1-k}{k}\right)^2\right]}$$  \hfill (1.22)

### 1.4.2 Variations of Currents and Voltages

Because the voltage across the inductor $L_2$ is $(V_2 - RI_2)$ during switch-on and $(V_1 - V_2 + V_C + RI_2)$ during switch-off, the average voltage across capacitor $C$ is

$$kT(V_2 - RI_2) = (V_1 - V_2 + V_C + RI_2)(1-k)T$$

Hence

$$V_C = \frac{V_2}{1-k} - V_1 - \frac{1}{1-k}RI_2 = \frac{V_2}{1-k} - V_1 - RI_1 \frac{k}{(1-k)^2}$$  \hfill (1.23)

The peak-to-peak variation of capacitor voltage $v_C$ is

$$\Delta v_C = \frac{Q_C}{C} = \frac{kT_1}{C} = \frac{kI_1}{fC}$$

The variation ratio of capacitor voltage $v_C$ is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{kI_1}{2fC \left[\frac{V_2}{1-k} - V_1 - RI_1 \frac{k}{(1-k)^2}\right]}$$  \hfill (1.24)

The peak-to-peak variation of current $i_{L_1}$ is

$$\Delta i_{L_1} = \frac{V_C - V_S - RI_1}{L_1}kT = \frac{V_2 - V_S - RI_2}{L_1}kT$$

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The variation ratio of inductor current $i_{L1}$ is

$$\xi_1 = \frac{\Delta i_{L1}}{I_{L1}} = \frac{k}{2fL_{I1}} \frac{V_2 - V_2 - RI_2}{L_1}$$ (1.25)

The peak-to-peak variation of inductor current $i_{L2}$ is

$$\Delta i_{L2} = \frac{V_2 - V_2 - RI_2}{L_2} kT$$

The variation ratio of inductor current $i_{L2}$ is

$$\xi_2 = \frac{\Delta i_{L2}}{I_{L2}} = \frac{k}{2fL_{I2}} \frac{V_2 - V_2 - RI_2}{L_2}$$ (1.26)

The free-wheeling diode’s current $i_{D1}$ during switch off is: $i_{D1} = i_{L1} + i_{L2}$. Its peak-to-peak variation is

$$\Delta i_{D1} = \Delta i_{L1} + \Delta i_{L2} = \frac{V_2 - V_2 - RI_2}{L} kT$$

where $L = L_1L_2 / (L_1 + L_2)$. The variation ratio of diode current $i_{D1}$ is

$$\xi_{D1} = \frac{\Delta i_{D1}}{I_{L1} + I_{L2}} = \frac{k}{2fL(I_1 + I_2)} \frac{V_2 - V_2 - RI_2}{2fL_{I2}}$$ (1.27)

### 1.4.3 Discontinuous Region

If the diode current becomes zero before $S_2$ is switched on again, the converter works in discontinuous region. The condition is: $\xi_{D1} = 1$, i.e.,

$$k^2 = \frac{2fL_{I2}}{V_2 - V_2 - RI_2}$$ (1.28)

From Equations (1.21) and (1.28) the boundary between continuous and discontinuous regions is shown in Figure 1.7. Particularly, since conduction duty $k$ is greater than $k_{min}$ and the current is high, the converter usually works in the continuous region.
1.5 Mode C (Quadrant III Operation)

As shown in Figure 1.4a and b the voltage across capacitor $C$ increases during switch-off, and decreases during switch on. Capacitor $C$ acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductor $L_1$. Assuming capacitor $C$ to be sufficiently large, the variation of the voltage across capacitor $C$ from its average value $V_C$ can be neglected in steady state, i.e., $v_C(t) = V_C$, even though it stores and transfers energy from the input to the output.

1.5.1 Circuit Description

The equivalent circuits in switch-on and -off states are shown in Figure 1.4a and b. When switch $S_1$ is on, the source current $i_1 = i_{L1}$. Inductor $L_1$ absorbs energy from the source. In the mean time inductor $L_2$ absorbs energy from capacitor $C$, current $i_{L1}$ increases and $i_2$ decreases. When switch $S_1$ is off, source current $i_1 = 0$. Current $i_{L1}$ flows through the free-wheeling diode $D_2$ to charge capacitor $C$ and increase current $i_2$. Inductor $L_1$ transfers its stored energy to capacitor $C$ and the load $V_2$. Current $i_{L1}$ decreases and $i_2$ increases. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 1.4c.

Actually, the variations of currents $i_{L1}$ and $i_{L2}$ are small so that $i_{L1} = I_{L1}$ and $i_{L2} = I_{L2} = i_2$.

Since the capacitor current $i_{C-off}$ is equal to $I_2$ during switch-on, $i_{C-off}$ should be:

$$i_{C-off} = \frac{k}{1-k} I_2$$  \hspace{1cm} (1.29)
Inductor current $i_{L1}$ during switch-off is

$$i_{L1} = I_2 + i_{C-off} = (1 + \frac{k}{1-k})I_2 = \frac{1}{1-k}I_2$$  \hspace{1cm} (1.30)$$

The source average current $I_1$ is

$$I_1 = ki_{L1} = \frac{k}{1-k}I_2 \quad \text{or} \quad I_{L1} = \frac{1}{k}I_1$$  \hspace{1cm} (1.31)$$

The input and output powers are

$$P_i = V_1I_1$$
and

$$P_o = V_2I_2$$

The power losses are

- $V_{S}I_1$ — Switch power loss
- $RI_{L1}^2$ — Power loss across inductor $L_1$
- $V_{D}I_1$ — Diode power loss
- $RI_{L2}^2$ — Power loss across inductor $L_2$

The total power losses are

$$P_{loss} = V_{S}I_1 + V_{D}I_1 + R(\frac{I_1^2}{k} + I_2^2)$$  \hspace{1cm} (1.32)$$

Since

$$P_i = P_o + P_{loss}$$

hence

$$V_1I_1 = V_2I_2 + (V_{S} + V_{D})I_1 + R(\frac{I_1^2}{k} + I_2^2)$$  \hspace{1cm} (1.33)$$

or

$$V_1 = V_2 \frac{1-k}{k} + (V_{S} + V_{D}) + RI_2\left[\frac{1}{k(1-k)} + \frac{1-k}{k}\right]$$  \hspace{1cm} (1.34)$$
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The output current is

\[
I_2 = \frac{V_1 - V_s - V_b - V_2}{R \left[ \frac{1}{k(1-k)} + \frac{1-k}{k} \right]}^{1-k \over k} \tag{1.35}
\]

The minimum conduction duty \( k \) corresponding to \( I_2 = 0 \) is

\[
k_{\text{min}} = \frac{V_2}{V_1 + V_2 - V_s - V_D} \tag{1.36}
\]

The power transfer efficiency is

\[
\eta_c = \frac{P_o}{P_i} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + \frac{V_s + V_D}{V_2} \frac{k}{1-k} + \frac{R I_2}{V_2} [1 + \left( \frac{1}{1-k} \right)^2]} \tag{1.37}
\]

1.5.2 Variations of Currents and Voltages

Because the voltage across the inductor \( L_1 \) is \((V_1 - RI_{L1})\) during switch-on and \((V_C + RI_{L1})\) during switch-off, the average voltage across capacitor \( C \) is

\[
kT(V_1 - RI_{L1}) = (V_C + RI_{L1})(1-k)T
\]

Hence

\[
V_C = \frac{k}{1-k} V_1 - \frac{1}{1-k} RI_{L1} = \frac{k}{1-k} V_1 - RI_2 \frac{1}{(1-k)^2} \tag{1.38}
\]

The peak-to-peak variation of capacitor voltage \( v_C \) is

\[
\Delta v_C = \frac{k I_2}{C} = \frac{k I_2}{fC}
\]

The variation ratio of capacitor voltage \( v_C \) is

\[
p = \frac{\Delta v_C / 2}{V_C} = \frac{k I_2}{2 f C \left[ \frac{k}{1-k} v_1 - \frac{R I_2}{(1-k)^2} \right]} \tag{1.39}
\]

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The peak-to-peak variation of inductor current \( i_{L1} \) is

\[
\Delta i_{L1} = \frac{V_1 - V_s - RI_1}{L_1} kT
\]

The variation ratio of inductor current \( i_{L1} \) is

\[
\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = k \frac{V_1 - V_s - RI_1}{2fL_1 I_1}
\]

Diode’s current \( i_{D2} \) during switch-off is: \( i_{D2} = i_{L1} \). Its peak-to-peak variation is

\[
\Delta i_{D2} = \Delta i_{L1} = \frac{V_1 - V_s - RI_1}{L_1} kT
\]

and the variation ratio of inductor current \( i_{D2} \) is

\[
\xi_{D2} = \xi_1 = \frac{\Delta i_{D2} / 2}{I_{L1}} = k \frac{V_1 - V_s - RI_1}{2fL_1 I_1}
\]

Since voltage \( v_C \) varies very little, the peak-to-peak variation of inductor current \( i_{L0} \) is calculated by the area \( A \) of a triangle with width \( T/2 \) and height \( \Delta v_C / 2 \):

\[
\Delta i_{L2} = A = \frac{1}{2} T \frac{kT L_2}{2} = \frac{k}{8f^2 C L_2} I_2
\]

The variation ratio of inductor current \( i_{L2} \) is

\[
\xi_2 = \frac{\Delta i_{L2} / 2}{I_2} = \frac{k}{16f^2 C L_2}
\]

### 1.5.3 Discontinuous Region

If the diode current becomes zero before \( S_1 \) is switched on again, the converter works in discontinuous region. The condition \( \xi_{D2} = 1 \), i.e.,

\[
k = \frac{2fL_1 I_1}{V_1 - V_s - RI_1}
\]
From Equations (1.36) and (1.42) the boundary between continuous and discontinuous regions is shown in Figure 1.8. Particularly, since conduction duty $k$ is greater than $k_{\text{min}}$ and the current is high, the converter usually works in the continuous region.

1.6 Mode D (Quadrant IV Operation)

As shown in Figure 1.5a and b the voltage across capacitor $C$ decreases during switch-on, and increases during switch off. Capacitor $C$ acts as the primary means of storing and transferring energy from the load battery to the source via inductor $L_1$. Assuming capacitor $C$ to be sufficiently large, the variation of the voltage across capacitor $C$ from its average value $V_C$ can be neglected in steady state, i.e., $v_C(t) = V_C$, even though it stores and transfers energy from the load $V_2$ to the source $V_1$.

1.6.1 Circuit Description

When switch $S_2$ is on, source current $i_1 = 0$. Current $i_{L1}$ flows through the switch $S_2$, then capacitor $C$ and load battery $V_2$. It increases and $i_{L1} = i_{C,\text{on}} + i_2$, when switch $S_2$ is off. The source current is $i_1 = i_{L1}$. The free-wheeling diode $D_1$ is conducted. Current $i_{L1}$ decreases. Inductor $L_1$ transfers its stored energy to source $V_1$. In order to analyze the circuit working process, these waveforms with enlarged variations are shown in Figure 1.5c. The equivalent circuits in switch-on and -off states are shown in Figure 1.5a and b.

Actually, the variations of currents $i_{L1}$ and $i_{L2}$ are small so that $i_{L1} \approx I_{L1}$ and $i_{L2} \approx I_2$. 

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Since the capacitor current $i_{C-off}$ is equal to $I_2$ during switch-off, $i_{C-on}$ should be:

$$i_{C-on} = \frac{1-k}{k}I_2$$  \hspace{1cm} (1.43)

Inductor current $i_{L1}$ during switch-on is

$$i_{L1} = I_2 + i_{C-off} = (1+\frac{1-k}{k})I_2 = \frac{1}{k}I_2$$  \hspace{1cm} (1.44)

The source average current $I_1$ is

$$I_1 = (1-k)i_{L1} = \frac{1-k}{k}I_2$$

or

$$I_{L1} = \frac{1}{1-k}I_1$$ \hspace{1cm} (1.45)

The input and output powers are

$$P_I = V_2I_2$$

and

$$P_O = V_1I_1$$

The power losses are

- $V_sI_1$ — Switch power loss
- $R_Ii_1^2$ — Power loss across inductor $L_1$
- $V_DI_1$ — Diode power loss
- $R_Ii_2^2$ — Power loss across inductor $L_2$

The total power losses are

$$P_{loss} = V_sI_1 + V_DI_1 + R(I_{L1}^2 + I_2^2)$$ \hspace{1cm} (1.46)

Since

$$P_I = P_O + P_{loss}$$

hence

$$V_2I_2 = V_1I_1 + (V_S + V_D)I_1 + R(I_{L1}^2 + I_2^2)$$ \hspace{1cm} (1.47)
or

\[ V_2 = \frac{1-k}{k} (V_i + V_S + V_D) + RI_1 \left[ \frac{1}{k(1-k)} + \frac{k}{1-k} \right] \] (1.48)

The output current is

\[ I_1 = \frac{V_2 - (V_i + V_S + V_D) \frac{1-k}{k}}{R \left[ \frac{1}{k(1-k)} + \frac{k}{1-k} \right]} \] (1.49)

The minimum conduction duty \( k \) corresponding to \( I_1 = 0 \) is

\[ k_{min} = \frac{V_i + V_S + V_D}{V_i + V_2 + V_S + V_D} \] (1.50)

The power transfer efficiency is

\[ \eta_D = \frac{P_O}{P_I} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + \frac{V_S + V_D}{V_1} + \frac{RI_1}{V_1} \left[ \frac{1}{(1-k)} + \left( \frac{k}{1-k} \right)^2 \right]} \] (1.51)

1.6.2 Variations of Currents and Voltages

Because the voltage across the inductor \( L_i \) is \((V_c - RI_{i1})\) during switch-on and \((V_i + RI_{i1})\) during switch-off, the average voltage across capacitor \( C \) is

\[ kT(V_c - RI_{i1}) = (V_i + RI_{i1})(1-k)T \]

Hence

\[ V_c = \frac{1-k}{k} V_i + \frac{1}{k} RI_{i1} = \frac{1-k}{k} V_i + RI_1 \frac{1}{k(1-k)} \] (1.52)

The peak-to-peak variation of capacitor voltage \( v_c \) is

\[ \Delta v_c = \frac{(1-k)TI_1}{C} = \frac{kI_1}{fC} \]

The variation ratio of capacitor voltage \( v_c \) is
The peak-to-peak variation of current $i_{L1}$ is

$$\Delta i_{L1} = kT \frac{V_c - V_s - RI_1}{L_1} = (1 - k) \frac{V_2 - V_s - RI_2}{fL_1}$$

The variation ratio of inductor current $i_{L1}$ is

$$\frac{\Delta i_{L1}}{I_{L1}} = \frac{\Delta i_{L1}}{2} = (1 - k) \frac{V_2 - V_s - RI_2}{2fL_1I_1}$$

Current $i_{D1}$ during switch-off is $i_{D1} = i_{L1}$. Its peak-to-peak variation is

$$\Delta i_{D1} = \Delta i_{L1} = (1 - k) \frac{V_2 - V_s - RI_2}{fL_1}$$

and the variation ratio of inductor current $i_{D1}$ is

$$\frac{\Delta i_{D1}}{I_{D1}} = \frac{\Delta i_{L1}}{I_{L1}} = \frac{\Delta i_{D1}}{2} = \frac{k}{fL_1I_2}$$

Since voltage $v_c$ varies very little, the peak-to-peak variation of inductor current $i_{L2}$ is calculated by the area $B$ of a triangle with width $T/2$ and height $\Delta v_c/2$:

$$\Delta i_{L2} = \frac{B}{L_2} = \frac{1}{2} \frac{T}{2} \frac{kI_1}{2CL_2} = \frac{k}{8f^2CL_2} I_1$$

The variation ratio of inductor current $i_{L2}$ is

$$\frac{\Delta i_{L2}}{I_{L2}} = \frac{\Delta i_{L2}}{2} = \frac{1 - k}{16f^2CL_2}$$

### 1.6.3 Discontinuous Region

If the diode current becomes zero before $S_2$ is switched on again, the converter works in discontinuous region. The condition is $\zeta_{D1} = 1$, i.e.,
From Equations (1.50) and (1.56) the boundary between continuous and discontinuous regions is shown in Figure 1.9. Particularly, since conduction duty $k$ is greater than $k_{min}$ and the current is high, the converter usually works in the continuous region.

### 1.7 Simulation Results

In order to verify the above analysis and calculation formulae, and the characteristics of this converter, we applied the PSpice simulation methodology to obtain the results shown in Figure 1.10 to Figure 1.13. The first plot is current $i_{L1}$, the second plot is current $i_{L2}$, and the third plot is voltage $v_C$. The repeating frequency $f = 50$ Hz. The conduction duty cycle $k = 0.4$ for modes A and C, 0.8 for modes B and D. These results agree with the analysis and calculations in the previous sections.

### 1.8 Experimental Results

In order to verify the above analysis and calculation formulae, and the characteristics of this converter, we collected the following experimental results. The experimental testing conditions are

$$k = \frac{2fL_1I_2}{V_2 - V_S - RI_2}$$

(1.56)
V₁ = 42 V, V₂ = 14 V, V₃ = 0.3 V, Vᵤ = 0.5 V, R = 0.05 Ω,

\[ L₁ = L₂ = L = Lₒ = 0.5 \text{ mH}, \quad C = 20 \mu\text{F}, \quad f = 50 \text{ kHz} \]

The experimental results corresponding to various conduction duty \( k \) are shown in Table 1.2 for the Mode A, Table 1.3 for the Mode B, Table 1.4 for the Mode C and Table 1.5 for the Mode D.

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When compared with the analysis and calculations, the experimental results are reasonable. From these data we can see that the function of this converter has been verified.
TABLE 1.2
The Experimental Results for Mode A (Quadrant Q₁) with \(k_{min} = 0.2536\)

<table>
<thead>
<tr>
<th>(k)</th>
<th>(I_1) (A)</th>
<th>(I_2) (A)</th>
<th>(V_C) (V)</th>
<th>(P_I) (W)</th>
<th>(P_o) (W)</th>
<th>(\eta_A) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.26</td>
<td>3.0</td>
<td>8.5</td>
<td>14.28</td>
<td>126</td>
<td>119</td>
<td>94.4</td>
</tr>
<tr>
<td>0.28</td>
<td>13.7</td>
<td>35.1</td>
<td>15.07</td>
<td>575</td>
<td>491</td>
<td>85.4</td>
</tr>
<tr>
<td>0.30</td>
<td>26.5</td>
<td>61.8</td>
<td>15.77</td>
<td>1113</td>
<td>865</td>
<td>77.7</td>
</tr>
<tr>
<td>0.32</td>
<td>41.5</td>
<td>88.2</td>
<td>16.33</td>
<td>1743</td>
<td>1235</td>
<td>70.8</td>
</tr>
<tr>
<td>0.34</td>
<td>58.8</td>
<td>114.2</td>
<td>18.77</td>
<td>2470</td>
<td>1599</td>
<td>64.7</td>
</tr>
</tbody>
</table>

TABLE 1.3
The Experimental Results for Mode B (Quadrant Q₂) with \(k_{min} = 0.7535\)

<table>
<thead>
<tr>
<th>(k)</th>
<th>(I_2) (A)</th>
<th>(I_1) (A)</th>
<th>(V_C) (V)</th>
<th>(P_I) (W)</th>
<th>(P_o) (W)</th>
<th>(\eta_B) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.76</td>
<td>8.81</td>
<td>2.78</td>
<td>13.70</td>
<td>123</td>
<td>117</td>
<td>94.9</td>
</tr>
<tr>
<td>0.78</td>
<td>35.72</td>
<td>10.08</td>
<td>12.72</td>
<td>500</td>
<td>423</td>
<td>84.6</td>
</tr>
<tr>
<td>0.80</td>
<td>62.0</td>
<td>15.5</td>
<td>11.67</td>
<td>870</td>
<td>652</td>
<td>75.0</td>
</tr>
<tr>
<td>0.82</td>
<td>87.7</td>
<td>19.3</td>
<td>10.57</td>
<td>1230</td>
<td>810</td>
<td>65.9</td>
</tr>
<tr>
<td>0.84</td>
<td>112.9</td>
<td>21.5</td>
<td>9.43</td>
<td>1580</td>
<td>903</td>
<td>57.1</td>
</tr>
</tbody>
</table>

TABLE 1.4
The Experimental Results for Mode C (Quadrant Q₃) with \(k_{min} = 0.2536\)

<table>
<thead>
<tr>
<th>(k)</th>
<th>(I_1) (A)</th>
<th>(I_2) (A)</th>
<th>(V_C) (V)</th>
<th>(P_I) (W)</th>
<th>(P_o) (W)</th>
<th>(\eta_C) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.26</td>
<td>3.0</td>
<td>8.5</td>
<td>14.28</td>
<td>126</td>
<td>119</td>
<td>94.4</td>
</tr>
<tr>
<td>0.28</td>
<td>13.7</td>
<td>35.1</td>
<td>15.07</td>
<td>575</td>
<td>491</td>
<td>85.4</td>
</tr>
<tr>
<td>0.30</td>
<td>26.5</td>
<td>61.8</td>
<td>15.77</td>
<td>1113</td>
<td>865</td>
<td>77.7</td>
</tr>
<tr>
<td>0.32</td>
<td>41.5</td>
<td>88.2</td>
<td>16.33</td>
<td>1743</td>
<td>1235</td>
<td>70.8</td>
</tr>
<tr>
<td>0.34</td>
<td>58.8</td>
<td>114.2</td>
<td>18.77</td>
<td>2470</td>
<td>1599</td>
<td>64.7</td>
</tr>
</tbody>
</table>

TABLE 1.5
The Experimental Results for Mode D (Quadrant Q₄) with \(k_{min} = 0.7535\)

<table>
<thead>
<tr>
<th>(k)</th>
<th>(I_2) (A)</th>
<th>(I_1) (A)</th>
<th>(V_C) (V)</th>
<th>(P_I) (W)</th>
<th>(P_o) (W)</th>
<th>(\eta_D)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.76</td>
<td>8.81</td>
<td>2.78</td>
<td>13.70</td>
<td>123</td>
<td>117</td>
<td>94.9</td>
</tr>
<tr>
<td>0.78</td>
<td>35.72</td>
<td>10.08</td>
<td>12.72</td>
<td>500</td>
<td>423</td>
<td>84.6</td>
</tr>
<tr>
<td>0.80</td>
<td>62.0</td>
<td>15.5</td>
<td>11.67</td>
<td>870</td>
<td>652</td>
<td>75.0</td>
</tr>
<tr>
<td>0.82</td>
<td>87.7</td>
<td>19.3</td>
<td>10.57</td>
<td>1230</td>
<td>810</td>
<td>65.9</td>
</tr>
<tr>
<td>0.84</td>
<td>112.9</td>
<td>21.5</td>
<td>9.43</td>
<td>1580</td>
<td>903</td>
<td>57.1</td>
</tr>
</tbody>
</table>
1.9 Discussion

1.9.1 Discontinuous-Conduction Mode

Usually, the industrial applications require that the DC/DC converters work in continuous mode. However, it is irresistible that DC/DC converter works in discontinuous mode sometimes. During switch-off if current $i_{D2}$ and $i_{D1}$ becomes zero before next period switch on, the state is called discontinuous mode. The following factors affect the diode current to become discontinuous:

1. Switching frequency $f$ is too low
2. Conduction duty cycle $k$ is too small and close $k_{min}$
3. Inductor $L$ is too small

1.9.2 Comparison with the Double-Output Luo-Converter

The analysis of the double output Luo-converter is based on ideal components. For example, all voltage drops are zero and inductor resistance is zero, i.e., $V_S = V_D = 0$ and $R = 0$. If we use these conditions the corresponding formulae will return back to those forms for double output Luo-converter. From Equation (1.5):

\[ k = \frac{V_2}{V_1 + V_2} \]

or

\[ V_2 = \frac{k}{1-k} V_1 \]

and

\[ I_2 = \frac{1-k}{k} I_1 \]

From Equation (1.19):

\[ k = \frac{V_1}{V_1 + V_2} \]
or

\[ V_1 = \frac{k}{1-k} V_2 \]

and

\[ I_1 = \frac{1-k}{k} I_2 \]

From Equation (1.34):

\[ k = \frac{V_2}{V_1 + V_2} \]

or

\[ V_2 = \frac{k}{1-k} V_1 \]

and

\[ I_2 = \frac{1-k}{k} I_1 \]

From Equation (1.48):

\[ k = \frac{V_1}{V_1 + V_2} \]

or

\[ V_1 = \frac{k}{1-k} V_2 \]

and

\[ I_1 = \frac{1-k}{k} I_2 \]

because the power losses are zero, the power transfer efficiency is 100\%.
1.9.3 Conduction Duty $k$

Since the source and load voltages are fixed, conduction duty $k$ does not affect the voltage transfer gain. We have considered the power losses on the switches, diodes, and inductors. Therefore, the conduction duty $k$ affects the output and input currents and power transfer efficiency. Usually, large $k$ causes large currents and power losses. For each mode there is a minimum conduction duty $k_{\text{min}}$. When $k = k_{\text{min}}$ the input and output currents are zero. In order to limit the overcurrent, the values of the conduction duty $k$ are usually selected in the range of

$$k_{\text{min}} < k < k_{\text{min}} + 0.12$$

1.9.4 Switching Frequency $f$

In this paper the repeating frequency $f = 50$ kHz was selected. Actually, switching frequency $f$ can be selected in the range between 10 kHz and 500 kHz. Usually, the higher the frequency, the lower the current ripples.

Bibliography

Switched Component Converters

Classic DC/DC converters consist of inductors and capacitors. They are large because of the mixture of inductors and capacitors. On engineering design experience, a circuit constructed by only inductor or capacitor may be small in size. In order to reduce the converter size and enlarge the power density, a third generation of DC/DC converters have been developed, and they are called switched component converters. Particularly, they are switched-capacitor (SC) DC/DC converters and switched-inductor (SI) DC/DC converters. The switched capacitor DC/DC converter is a new prototype of DC/DC conversion technology. Since a switched capacitor can be integrated into a power IC chip, these converters are small and have a high power density. However, most of the published papers avoid discussing the efficiency because most switched capacitor converters possess low power transfer efficiency. This section introduces a switched capacitor two-quadrant DC/DC converter implementing voltage lift and current amplification techniques with high efficiency, high power density, and low electromagnetic interference (EMI). Experimental results verified the advantages of this converter. Four-quadrant operation is required by industrial applications. SC converters can perform four-quadrant operations as well.

SC converters always perform in push-pull state, and the control circuitry is complex. A large number of capacitors are required, especially in the case of large differences between input and output voltages.

Switched inductor DC/DC converters are a prototype of DC/DC conversion technology from SC converters. Switched inductor DC/DC converters have advantages such as simple structure, simple control circuitry, high efficiency, large power, and high power density. Usually, one inductor is required for a SI DC/DC converter. Since it consists of only an inductor, it is small. This converter has advantages: no matter how many quadrant operations and how large the difference between input and output voltages, only one inductor is usually employed in one SI DC/DC converter.
2.1 Introduction

A new type DC/DC converter consisting of capacitors only was developed around the 1980s. Since it can be integrated into a power semiconductor IC chip, it has attracted much attention in recent years. However, most of the converters introduced in the literature perform single-quadrant operations. Some of them work in the flip-flop status, and their control circuit and topologies are very complex.

A newly designed DC/DC converter, two-quadrant DC/DC converter with switched capacitors was developed from the prototype of the authors’ research work. This converter implements the voltage-lift and current-amplification technique, so that it reaches high power density and high power transfer efficiency. In order to successfully reduce electromagnetic interference (EMI), a lower switching frequency $f = 5$ kHz was applied in this converter. It can perform step-down and step-up two-quadrant positive to positive DC/DC voltage conversion with high power density, low EMI, and cheap topology in simple structure.

The conduction duty $k$ is usually selected to be $k = 0.5$ in most of the papers in the literature. We have carefully analyzed this problem, and verified its reasonableness.

Multiple-quadrant operation is required by industrial applications. Switched-capacitor multiple quadrant converters and switched inductor multiple quadrant converters will be introduced in this chapter as well.

2.2 A Two-Quadrant SC DC/DC Converter

A two-quadrant SC converter is shown in Figure 2.1. It consists of nine switches, seven diodes, and three capacitors. The high voltage (HV) source and low voltage (LV) load are usually constant voltages. The load can be a battery or motor back electromotive force (EMF). For example, the source voltage is 48 V and load voltage is 14 V. There are two modes of operation:

1. Mode A (quadrant I): electrical energy is transferred from HV side to LV side;
2. Mode B (quadrant II): electrical energy is transferred from LV side to HV side.

2.2.1 Circuit Description

Each mode has two states: on and off. Usually, each state operates in different conduction duty $k$. The switching period is $T$ where $T = 1/f$. The parasitic
resistance of all switches is $r_s$, the equivalent resistance of all capacitors is $r_c$ and the equivalent voltage drop of all diodes is $V_D$. Usually select the three capacitors have same capacitance $C_1=C_2=C_3=C$. Some reference data are useful: $r_s=0.03 \, \Omega$, $r_c=0.02 \, \Omega$, and $V_D=0.5 \, V$. Here, $f=5 \, kHz$, and $C=5000 \, \mu F$.

### 2.2.1.1 Mode A

For mode A, state-on is shown in Figure 2.2a: switches $S_1$ and $S_{10}$ are closed and diodes $D_5$ and $D_5$ are conducting. Other switches and diodes are open. In this case capacitors $C_1$, $C_2$, and $C_3$ are charged via the circuit $V_H-S_1-C_1-D_5-C_2-D_6-C_3-S_{10}$ and the voltage across capacitors $C_1$, $C_2$, and $C_3$ is increasing. The equivalent circuit resistance is $R_{AN}=(2r_s+3r_c)=0.12 \, \Omega$, and the voltage deduction is $2V_D=1 \, V$. State-off is shown in Figure 2.2b: switches $S_2$, $S_3$, and $S_4$ are closed and diodes $D_6$, $D_8$, and $D_9$ are conducting. Other switches and diodes are open. In this case capacitor $C_1$ ($C_2$ and $C_3$) is discharged via the circuit $S_2(S_3$ and $S_4)-V_L-D_8(D_9$ and $D_{10})-C_1(C_2$ and $C_3)$, and the voltage across capacitor $C_1$ ($C_2$ and $C_3$) is decreasing. The equivalent circuit resistance is $R_{AF}=r_s+r_c=0.05 \, \Omega$, and the voltage deduction is $V_D=0.5 \, V$. Capacitors $C_1$, $C_2$, and $C_3$ transfer the energy from the source to the load. The voltage waveform across capacitor $C_1$ is shown in Figure 2.2c.

Mode A uses the current-amplification technique. All three capacitors are charged in series during state-on. The input current flows through three capacitors and the charges accumulated on the three capacitors should be the same. These three capacitors are discharged in parallel during state-off. Therefore, the output current is amplified by three.

### 2.2.1.2 Mode B

For mode B, state-on is shown in Figure 2.3a: switches $S_8$, $S_9$, and $S_{10}$ are closed and diodes $D_8$, $D_9$, and $D_{10}$ are conducting. Other switches and diodes are off. In this case all three capacitors are charged via each circuit $V_L-D_8(D_8$ and $D_{10})-C_1(C_2$ and $C_3)-S_8(S_9$ and $S_{10})$, and the voltage across three capacitors...
is increasing. The equivalent circuit resistance is $R_{BN} = r_s + r_c$ and the voltage deduction is $V_D$. State-off is shown in Figure 2.3b: switches $S_5$, $S_6$, and $S_7$ are closed and diode $D_1$ is on. Other switches and diodes are open. In this case all capacitors are discharged via the circuit $V_L - S_7 - C_3 - S_6 - C_2 - S_5 - C_1 - D_1 - V_H$ and the voltage across all capacitors is decreasing. The equivalent circuit resistance is $R_{BF} = 3 \ (r_s + r_c)$ and the voltage deduction is $V_D$. The voltage waveform across capacitor $C_1$ is shown in Figure 2.3c.

Mode B implements the voltage-lift technique. All three capacitors are charged in parallel during state-on. The input voltage is applied to the three

---

**FIGURE 2.2**
Mode A operation.
capacitors symmetrically, so that the voltages across these three capacitors should be the same. They are discharged in series during state-off. Therefore, the output voltage is lifted by three.

**Summary.** In this circuit we have $$R_{AN} = 0.12 \, \Omega$$, $$R_{AF} = 0.05 \, \Omega$$, $$R_{BN} = 0.05 \, \Omega$$, $$R_{BF} = 0.15 \, \Omega$$. The switch status is shown in Table 2.1.

### 2.2.2 Mode A (Quadrant I Operation)

Refer to Figure 2.2a and b the voltage across capacitor $$C_1$$ increases during switch-on, and decreases during switch-off according to the integration of the current $$i_{C1}$$. If the switching period $$T$$ is small enough (comparing with the circuit time constant) we can use average current to replace its instantaneous value for the integration. Therefore the voltage across capacitor $$C_1$$ is
The current flowing through the three capacitors is an exponential function. If the switching period $T$ is small enough (comparing with the circuit time constant) we can use their initial values while ignoring their variations. Therefore the current flowing through capacitor $C_1$ is

$$i_{c1}(t) = \begin{cases} v_{c1}(0) + \frac{1}{C} \int_0^t i_{c1}(t)dt = v_{c1}(0) + \frac{t}{C}i_H & 0 \leq t < kT \\ v_{c1}(kT) + \frac{1}{C} \int_{kT}^t i_{c1}(t)dt = v_{c1}(kT) - \frac{t-kT}{C}i_L & kT \leq t < T \end{cases} \quad (2.1)$$

The variation of the voltage across capacitor $C_1$ is

$$v_{c1}(t) = \begin{cases} \frac{V_H - 3v_{c1}(0) - 2V_D}{R_{AN}}(1 - e^{-t/R_{AN}C}) = \frac{V_H - 3V_{C1} - 2V_D}{R_{AN}} = i_H & 0 \leq t < kT \\ \frac{v_{c1}(kT) - V_L - V_D}{R_{AF}}e^{-t/R_{AF}C} = -\frac{V_{C1} - V_L - V_D}{R_{AF}} = -i_L & kT \leq t < T \end{cases} \quad (2.2)$$

Therefore,

$$i_H = 3\frac{1-k}{k}i_L \quad (2.3)$$

Where $i_H$ is the average input current in the switch-on period $kT$ that is equal to $I_{ih}/k$, and $i_L$ is the average output current in the switch-off period $(1-k)T$ that is equal to $I_{l}/3(1-k)$. Therefore, we have $3i_H = I_{l}$.

The variation of the voltage across capacitor $C_1$ is

**TABLE 2.1**

<table>
<thead>
<tr>
<th>Switches and Diodes</th>
<th>Mode A</th>
<th>Mode B</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>$D_1$</td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>$S_2S_3S_4$</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>$D_2D_3D_4$</td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>$S_5S_6S_7$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$D_5D_6$</td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>$S_8S_9$</td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>$S_{10}$</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>$D_8D_9D_{10}$</td>
<td></td>
<td>ON</td>
</tr>
</tbody>
</table>

*Note:* The blank status means off.
\[
\Delta v_{C1} = \frac{1}{C} \int_0^{kT} i_{C1}(t)dt = \frac{kT}{C} I_H = \frac{k(V_H - 3V_{C1} - 2V_D)}{f_{CRC}} \\
0 \leq t < kT
\]

or
\[
\Delta v_{C1} = \frac{1}{C} \int_{kT}^{T} i_{C1}(t)dt = \frac{(1-k)T}{C} I_L = \frac{(1-k)(V_{C1} - V_L - V_D)}{f_{CRC}} \\
kT \leq t < (1-k)T
\]

After calculation,
\[
V_{C1} = \frac{k(V_H - 2V_D) + 2.4(1-k)(V_L + V_D)}{2.4 + 0.6k}
(2.4)
\]

Hence
\[
\Delta v_{C1} = \frac{k(V_H - 3V_{C1} - 2V_D)}{f_{CRC}} = \frac{2.4k(1-k)(V_H - 3V_L - 5V_D)}{(2.4 + 0.6k)f_{CRC}}
(2.5)
\]

We have
\[
v_{C1}(0) = V_{C1} - \frac{\Delta v_{C1}}{2} \quad \text{and} \quad v_{C1}(kT) = V_{C1} + \frac{\Delta v_{C1}}{2}
\]

The average output current is
\[
I_L = \frac{3}{T} \int_{kT}^{T} i_{C1}(t)dt = 3(1-k) \frac{V_{C1} - V_L - V_D}{R_{AF}}
(2.6)
\]

The average input current is
\[
I_H = \frac{1}{T} \int_0^{kT} i_{C1}(t)dt = k \frac{V_H - 3V_{C1} - 2V_D}{R_{AN}}
(2.7)
\]

Output power is
\[
P_O = V_L I_L = 3(1-k)V_L \frac{V_{C1} - V_L - V_D}{R_{AF}}
(2.8)
\]
Input power is

\[ P_I = V_H I_H = k V_H \frac{V_H - 3 V_{C1} - V_D}{R_{AN}} \]  

(2.9)

The transfer efficiency is

\[ \eta_A = \frac{P_D}{P_I} = \frac{1 - k}{k} \frac{3 V_{AN}}{V_H \frac{V_H - 3 V_{C1} - V_D}{R_{AN}}} \]

(2.10)

If \( f = 5 \text{ kHz} \), \( V_H = 48 \text{ V} \) and \( V_L = 14 \text{ V} \), and all \( C = 5000 \mu\text{F} \), for the various \( k \) values, the data are shown in Table 2.2.

From this analysis, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent upon \( R \), \( C \), \( f \), and \( k \). The conduction duty \( k \) does not affect the power transfer efficiency, it affects the input and output power in a small region. The maximum output power corresponds at \( k = 0.5 \).

### 2.2.3 Mode B (Quadrant II Operation)

Refer to Figure 2.3a and b, the voltage across capacitor \( C_1 \) increases during switch-on, and decreases during switch-off according to the integration of the current \( i_{C1} \). If the switching period \( T \) is small enough we can use average current to replace its instantaneous value for the integration. Therefore the voltage across capacitor \( C_1 \) is

\[ v_{C1}(t) = \begin{cases} 
0 & \quad 0 \leq t < kT \\
\frac{1}{C} \int_0^t i_{C1}(t)dt = v_{C1}(0) + \frac{t}{C} I_L & \quad 0 \leq t < kT \\
\frac{1}{C} \int_{kT}^t i_{C1}(t)dt = v_{C1}(kT) - \frac{t - kT}{C} I_H & \quad kT \leq t < T 
\end{cases} \]

(2.11)

The current flowing through the three capacitors is an exponential function. If the switching period \( T \) is small enough we can use their initial values and ignore their variations. Therefore the current flowing through capacitor \( C_1 \) is

\[ P_I = V_H I_H = k V_H \frac{V_H - 3 V_{C1} - V_D}{R_{AN}} \]
\[ i_{C1}(t) = \left\{ \begin{array}{ll}
\frac{V_L - v_{C1}(0) - V_D}{R_{BN}} \left( 1 - e^{-1/R_{BN}C} \right) + \frac{V_L - V_{C1} - V_D}{R_{BN}} \approx -\frac{i_L}{R_{BN}} & 0 \leq t \leq kT \\
-\frac{3V_C}{R_{BF}} + V_L - V_H - V_D - \frac{3V_C + V_L - V_H - V_D}{R_{BF}} = -\frac{i_H}{R_{BF}} & kT \leq t \leq T
\end{array} \right. \] (2.12)

Therefore,
\[ \bar{i}_L = \frac{1-k}{k} \bar{i}_H \] (2.13)

Where \( \bar{i}_L \) is the average input current in the switch-on period \( kT \) that is equal to \( I_L/k \), and \( \bar{i}_H \) is the average output current in the switch-off period \( (1-k)T \) that is equal to \( I_H/3(1-k) \). Therefore, we have \( 4I_H = I_L \).

The variation of the voltage across capacitor \( C \) is
\[ \Delta v_{C1} = \frac{1}{C} \int_{0}^{kT} i_{C1}(t)dt = \frac{kT}{C} \bar{i}_L = \frac{k(V_L - V_{C1} - V_D)}{fCR_{BN}} \] \( \leq kT \)

or
\[ \Delta v_{C1} = \frac{1}{C} \int_{kT}^{T} i_{C1}(t)dt = \frac{(1-k)T}{C} \bar{i}_H = \frac{(1-k)(3V_C + V_L - V_H - V_D)}{fCR_{BF}} \] \( kT \leq (1-k)T \)

After calculation,
\[ V_{C1} = k(V_L - V_D) + \frac{1-k}{3}(V_H - V_L + V_D) \] (2.14)

Hence
\[ \Delta v_{C1} = \frac{k(1-k)[4(V_L - V_D) - V_H]}{fCR_{BN}} \] (2.15)

\[ v_{C1}(0) = V_{C1} - \frac{\Delta v_{C1}}{2} \quad \text{and} \quad v_{C1}(kT) = V_{C1} + \frac{\Delta v_{C1}}{2} \]
The average input current is

\[
I_L = \frac{1}{T} \left[ 3 \int_{0}^{T} i_{C1}(t) dt + \int_{\frac{1}{2}T}^{T} i_{C1}(t) dt \right] = 3k \frac{V_L - V_{C1} - V_D}{R_{BN}} + (1 - k) \frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} \tag{2.16}
\]

The average output current is

\[
I_H = \frac{1}{T} \int_{\frac{1}{2}T}^{T} i_{C1}(t) dt = (1 - k) \frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} \tag{2.17}
\]

Input power is

\[
P_I = V_L I_L = V_L \left[ 3k \frac{V_L - V_{C1} - V_D}{R_{BN}} + (1 - k) \frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} \right] \tag{2.18}
\]

Output power is

\[
P_O = V_H I_H = V_H (1 - k) \frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} \tag{2.19}
\]

The transfer efficiency is

\[
\eta_b = \frac{P_O}{P_I} = \frac{V_H}{4V_L} \tag{2.20}
\]

If \( f = 5 \text{ kHz} \), \( V_H = 48 \text{ V} \) and \( V_L = 14 \text{ V} \), and all \( C = 5000 \mu \text{F} \), for the various \( k \) values the data are shown in Table 2.3.

From this analysis, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of \( R \), \( C \), \( f \), and \( k \). The conduction duty \( k \) does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds at \( k = 0.5 \).
2.2.4 Experimental Results

A two-quadrant DC/DC converter operates the conversion between 14 V and 48 VDC. The converter has been developed and is introduced in this paper. This converter is a two-quadrant DC/DC converter with switched-capacitors for the dual-direction conversion between 14 V and 48 VDC. A testing rig was constructed and consists of a modern car battery 14 VDC as a load and a 48 VDC source power supply. The testing conditions are

- Switching frequency: $f = 5 \text{ kHz}$
- Conduction duty: $k = 0.5$
- High and low voltages: $V_{H} = 48 \text{ V}$ and $V_{L} = 14 \text{ V}$
- All capacitance: $C = 5000 \mu\text{F}$

The experimental results are shown in Table 2.4. The average power transfer efficiency is 85%. The total average power density (PD) is 16.7 W/in³. This figure is much higher than the PD of classical converters, which are usually less than 5 W/in³. Since the switching frequency is low, the electromagnetic interference (EMI) is weak.

### Table 2.4

<table>
<thead>
<tr>
<th>Mode</th>
<th>$I_{L}$ (A)</th>
<th>$I_{H}$ (A)</th>
<th>$V_{C}$ (V)</th>
<th>$P_{L}$ (W)</th>
<th>$P_{H}$ (W)</th>
<th>$\eta$ (%)</th>
<th>$\overline{P}$ (W)</th>
<th>Volume (in³)</th>
<th>PD (W/in³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>18.9</td>
<td>6.4</td>
<td>15.15</td>
<td>307</td>
<td>264</td>
<td>86</td>
<td>286</td>
<td>24</td>
<td>11.9</td>
</tr>
<tr>
<td>B</td>
<td>40</td>
<td>9.8</td>
<td>12.5</td>
<td>560</td>
<td>470</td>
<td>84</td>
<td>515</td>
<td>24</td>
<td>21.5</td>
</tr>
<tr>
<td>Average</td>
<td>29.45</td>
<td>8.1</td>
<td>13.8</td>
<td>434</td>
<td>367</td>
<td>85</td>
<td>400</td>
<td>24</td>
<td>16.7</td>
</tr>
</tbody>
</table>

2.2.5 Discussion

2.2.5.1 Efficiency

From theoretical analysis and experimental results we find that the power transfer efficiency of switched capacitor converters is limited. The reason to spoil the power transfer efficiency is the power consumption on the circuit parasitic resistors and the diodes.

In steady state, the increase and decrease of the charge across a capacitor should be equal to each other. Therefore, its average input current $I_{i}$ must be equal to the average output current $I_{o}$. If only one capacitor is applied in a switched capacitor DC/DC converter, its power transfer efficiency is

$$\eta = \frac{P_{O}}{P_{I}} = \frac{V_{O}I_{O}}{V_{I}I_{I}} = \frac{V_{O}}{V_{I}}$$

(2.21)
Since the voltage-lift and current-amplification technique are applied in the circuit, the power transfer efficiency is around 86.6%, which is much higher than those of the circuits introduced by the literature.

2.2.5.2 Conduction Duty $k$
From the data calculated in previous sections, it can be seen that if $k = 0.4$, 0.5, or 0.6 the efficiencies $\eta_A$ and $\eta_B$ are not changed. The output power is slightly affected by $k$, and its maximum value corresponds $k = 0.5$. Therefore, we can take the typical data corresponding to $k = 0.5$.

2.2.5.3 Switching Frequency $f$
Because the switching frequency $f = 5$ kHz is very low, its electromagnetic interference (EMI) is much lower than that of the traditional classical converters. The switching frequency applied in the traditional classical converters normally ranges between 50 kHz to 200 kHz.

2.3 Four-Quadrant Switched Capacitor DC/DC Luo-Converter
Since most SC DC/DC converters published in the literature perform in single-quadrant operation working in the push-pull status their control circuit and topologies are very complex. This section introduces an SC four-quadrant DC/DC Luo-converter. The experimental results verified our analysis and calculation. This converter, shown in Figure 2.4, consists of eight switches and two capacitors. The source voltage $V_1$ and load voltage $V_2$ (e.g., a battery or DC motor back EMF) are usually constant voltages. In this paper they are assumed to be 21 V and 14 V. Capacitors $C_1$ and $C_2$ are the same and $C_1 = C_2 = 2000 \, \mu F$. The circuit equivalent resistance $R = 50 \, \text{m}\Omega$. Therefore, there are four modes of operation for this converter:
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Mode A (quadrant I, Q I): energy is transferred from source to positive voltage load

Mode B (quadrant II, Q II): energy is transferred from positive voltage load to source

Mode C (quadrant III, Q III): energy is transferred from source to negative voltage load

Mode D (quadrant IV, Q IV): energy is transferred from negative voltage load to source

The first quadrant is called the forward motoring (Forw. Mot.) operation. \( V_1 \) and \( V_2 \) are positive, and \( I_1 \) and \( I_2 \) are positive as well. The second quadrant is called the forward regenerative (Forw. Reg.) braking operation. \( V_1 \) and \( V_2 \) are positive, and \( I_1 \) and \( I_2 \) are negative. The third quadrant is called the reverse motoring (Rev. Mot.) operation. \( V_1 \) and \( I_1 \) are positive, and \( V_2 \) and \( I_2 \) are negative. The fourth quadrant is called the reverse regenerative (Rev. Reg.) braking operation. \( V_1 \) and \( I_1 \) are positive, and \( V_2 \) and \( I_2 \) are negative.

Each mode has two conditions: \( V_1 > V_2 \) and \( V_1 < V_2 \). Each condition has two states: \( \text{on} \) and \( \text{off} \). Usually, each state operates in a different conduction duty \( k \). The switching period is \( T \) where \( T = 1/f \). The switch status is shown in Table 2.5.

For mode A1, condition \( V_1 > V_2 \) is shown in Figure 2.5. Since \( V_1 > V_2 \) two capacitors C1 and C2 can be used in parallel. During switch on state, switches \( S_{1a}, S_{4a}, S_{6a}, \) and \( S_3 \) are closed and other switches are open. In this case capacitors \( C_1/C_2 \) are charged via the circuit \( V_1−S_{1a}−C_{1a}/C_{2a}−S_3 \), and the voltage across capacitors \( C_1 \) and \( C_2 \) is increasing. During switch off state, switches \( S_{2a}, S_{4a}, \) and \( S_8 \) are closed and other switches are open. In this case capacitors \( C_1/C_2 \) are discharged via the circuit \( S_2−V_2−S_8−C_{1a}/C_{2a} \), and the voltage across capacitors \( C_1 \) and \( C_2 \) is decreasing. Capacitors \( C_1 \) and \( C_2 \) transfer the energy from the source to the load. The voltage waveform across capacitor \( C_1 \) is shown in Figure 2.5c.

Note: Omitted switches are off.

<table>
<thead>
<tr>
<th>Q No</th>
<th>Condition</th>
<th>ON</th>
<th>OFF</th>
<th>Source</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>( V_1 &gt; V_2 )</td>
<td>( S_{1a}, S_{4a}, S_{6a}, S_3 )</td>
<td>( S_{2a}, S_{4a}, S_8 )</td>
<td>( V_1^+ )</td>
<td>( V_2^+ )</td>
</tr>
<tr>
<td>B</td>
<td>( V_1 &lt; V_2 )</td>
<td>( S_{1a}, S_{4a}, S_{6a}, S_3 )</td>
<td>( S_{2a}, S_{4a} )</td>
<td>( I_1^+ )</td>
<td>( I_2^+ )</td>
</tr>
<tr>
<td>C</td>
<td>( V_1 &gt;</td>
<td>V_2</td>
<td>)</td>
<td>( S_{1a}, S_{4a}, S_{6a}, S_3 )</td>
<td>( S_{2a}, S_{4a} )</td>
</tr>
<tr>
<td>D</td>
<td>( V_1 &lt;</td>
<td>V_2</td>
<td>)</td>
<td>( S_{1a}, S_{4a}, S_{6a}, S_3 )</td>
<td>( S_{2a}, S_{4a} )</td>
</tr>
</tbody>
</table>

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For mode A2, condition $V_1 < V_2$ is shown in Figure 2.6. Since $V_1 < V_2$, two capacitors $C_1$ and $C_2$ are in parallel during switch-on and in series during switch-off. This is the voltage lift technique. During switch-on state, switches $S_1, S_4, S_6, S_8$ are closed and other switches are open. In this case capacitors $C_1$ and $C_2$ are charged via the circuit $V_1 - S_1 - C_1/C_2 - S_4$, and the voltage across capacitors $C_1$ and $C_2$ is increasing. During switch-off state, switches $S_2, S_4, S_6, S_8$ are closed and other switches are open. In this case capacitors $C_1$ and $C_2$ are discharged via the circuit $S_2 - V_2 - S_4 - C_1 - S_7 - C_2$, and the voltage across capacitor $C_1$ and $C_2$ is decreasing. Capacitors $C_1$ and $C_2$ transfer the energy from the source to the load. The voltage waveform across capacitor $C_1$ is shown in Figure 2.6c.

For mode B1, condition $V_1 > V_2$ is shown in Figure 2.7. Since $V_1 > V_2$, two capacitors $C_1$ and $C_2$ are in parallel during switch-on and in series during switch-off. The voltage lift technique is applied. During switch-on state, switches $S_2, S_4, S_6, S_8$ and $S_3$ are closed. In this case capacitors $C_1/C_2$ are charged via the circuit $V_2 - S_2 - C_1/C_2 - S_4$, and the voltage across...
capacitors $C_1$ and $C_2$ is increasing. During switch-off state, switches $S_4$, $S_7$ and $S_3$ are closed. In this case capacitors $C_1$ and $C_2$ are discharged via the circuit $S_3-V_1-S_4-C_2-S_7-S_3$, and the voltage across capacitor $C_1$ and $C_2$ is decreasing. Capacitors $C_1$ and $C_2$ transfer the energy from the load to the source. The voltage waveform across capacitor $C_1$ is shown in Figure 2.7c.

For mode B2, condition $V_1 < V_2$ is shown in Figure 2.8. Since $V_1 < V_2$ two capacitors $C_1$ and $C_2$ can be used in parallel. During switch-on state, switches $S_1$, $S_6$, $S_4$, and $S_8$ are closed. In this case capacitors $C_1/C_2$ are charged via the circuit $V_1-S_1-C_1/C_2-S_6$, and the voltage across capacitors $C_1$ and $C_2$ is increasing. During switch-off state, switches $S_1$, $S_6$, $S_4$, and $S_8$ are closed. In this case capacitors $C_1/C_2$ are discharged via the circuit $S_1-V_1-S_6-C_1/C_2$, and the voltage across capacitors $C_1$ and $C_2$ are decreasing. Capacitors $C_1$ and $C_2$ transfer the energy from the load to the source. The voltage waveform across capacitor $C_1$ is shown in Figure 2.8c.

For mode C1, condition $V_1 > |V_2|$ is shown in Figure 2.9. Since $V_1 > |V_2|$ two capacitors $C_1$ and $C_2$ can be used in parallel. During switch-on state, switches $S_1$, $S_6$, $S_4$, and $S_8$ are closed. In this case capacitors $C_1/C_2$ are charged via the circuit $V_1-S_1-C_1/C_2-S_6$, and the voltage across capacitors $C_1$ and $C_2$ is increasing. During switch-off state, switches $S_1$, $S_6$, $S_4$, and $S_8$ are closed. In this case capacitors $C_1/C_2$ are discharged via the circuit $S_1-V_1-S_6-C_1/C_2$, and the voltage across capacitors $C_1$ and $C_2$ are decreasing. Capacitors $C_1$ and $C_2$ transfer the energy from the load to the source.
C₁ and C₂ is increasing. During switch-off state, switches S₃, S₅, S₆, and S₈ are closed. Capacitors C₁ and C₂ are discharged via the circuit S₅–V₂–S₆–C₁//C₂ and the voltage across capacitors C₁ and C₂ is decreasing. Capacitors C₁ and C₂ transfer the energy from the source to the load. The voltage waveform across capacitor C₁ is shown in Figure 2.9c.

For mode C2, condition $V_1 < |V_2|$ is shown in Figure 2.10. Since $V_1 < |V_2|$ two capacitors C₁ and C₂ are in parallel during switch-on and in series during switch-off, applying the voltage lift technique. During switch-on state, switches S₃, S₅, S₆, and S₈ are closed. Capacitors C₁ and C₂ are charged via the circuit $V₁–S₃–C₁//C₂–S₈$ and the voltage across capacitors C₁ and C₂ is increasing. During switch-off state, switches S₃, S₅, and S₇ are closed. Capacitors C₁ and C₂ are discharged via the circuit $S₃–V₂–S₅–C₁–S₇–C₂$ and the voltage across capacitor C₁ and C₂ is decreasing. Capacitors C₁ and C₂ transfer the energy from the source to the load. The voltage waveform across capacitor C₁ is shown in Figure 2.10c.

For mode D₁, condition $V_1 > |V_2|$ is shown in Figure 2.11. Since $V_1 > |V_2|$ two capacitors C₁ and C₂ are in parallel during switch-on and in series
during switch-off, applying the voltage lift technique. During switch-on state, switches $S_3$, $S_5$, $S_6$, and $S_8$ are closed. In this case capacitors $C_1/C_2$ are charged via the circuit $V_2 - S_3 - C_1/C_2 - S_5$, and the voltage across capacitors $C_1$ and $C_2$ is increasing. During switch-off state, switches $S_1$, $S_4$, and $S_7$ are closed. Capacitors $C_1$ and $C_2$ are discharged via the circuit $S_1 - V_1 - S_4 - C_1/C_2 - S_7$, and the voltage across capacitor $C_1$ and $C_2$ is decreasing. Capacitors $C_1$ and $C_2$ transfer the energy from the load to the source. The voltage waveform across capacitor $C_1$ is shown in Figure 2.11c.

For Mode D2, condition $V_1 < |V_2|$ is shown in Figure 2.12. Since $V_1 < |V_2|$ two capacitors $C_1$ and $C_2$ can be used in parallel. During switch-on state, switches $S_3$, $S_5$, $S_6$, and $S_8$ are closed. In this case capacitors $C_1/C_2$ are charged via the circuit $V_2 - S_3 - C_1/C_2 - S_5$, and the voltage across capacitors $C_1$ and $C_2$ is increasing. During switch-off state, switches $S_1$, $S_4$, $S_6$, and $S_8$ are closed. Capacitors $C_1$ and $C_2$ are discharged via the circuit $S_1 - V_1 - S_4 - C_1/C_2 - S_7$, and the voltage across capacitors $C_1$ and $C_2$ is decreasing. Capacitors $C_1$ and $C_2$ transfer the energy from the load to the source. The voltage waveform across capacitor $C_1$ is shown in Figure 2.12c.
2.3.1 Mode A (Q₁: Forward Motoring)

2.3.1.1 Mode A₁: Condition $V_1 > V_2$

Mode A₁, condition $V_1 > V_2$, is shown in Figure 2.5. Because two capacitors are connected in parallel, the total capacitance is $C = C_1 + C_2 = 4000 \, \mu F$. Suppose that the equivalent circuit resistance is $R = 50 \, \text{mΩ}$, $V_1 = 21 \, \text{V}$ and $V_2 = 14 \, \text{V}$, and the switching frequency is $f = 5 \, \text{kHz}$. The voltage and current across the capacitors are

$$v_c(t) = \begin{cases} 
  v_c(0) + \frac{1}{C} \int_0^t i_c(t) dt = v_c(0) + \frac{t}{C_1} & 0 \leq t < kT \\
  v_c(kT) + \frac{1}{C} \int_{kT}^t i_c(t) dt = v_c(kT) - \frac{t - kT}{C_2} & kT \leq t < T 
\end{cases}$$

(2.22)
Therefore, \( I_1 = \frac{1-k}{k} I_2 \) (2.24)

Where \( \overline{I}_1 \) is the average input current in the switch-on period \( kT \) that is equal to \( I_1/k \), and \( \overline{I}_2 \) is the average output current in the switch-off period \((1-k)T\) that is equal to \( I_2/(1-k) \). Therefore, we have \( I_1 = I_2 \). The variation of the voltage across capacitor \( C \) is
After calculation,\[ V_c = kV_1 + (1-k)V_2 \] (2.25)

Hence

\[ V_c = kV_1 + (1-k)V_2 \]
We then have

\[ \Delta v_C = \frac{k(1-k)(V_1 - V_2)}{fCR} \]  \hspace{1cm} (2.26)

We then have

\[ v_c(0) = V_C - \frac{\Delta v_C}{2} \]

and

\[ v_c(kT) = V_C + \frac{\Delta v_C}{2} \]

The average output current is

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Output power is

\[ P_0 = V_1 I_2 = (1-k)V_2 \frac{V_C - V_2}{R} \]  \hspace{1cm} (2.29)

Input power is

\[ P_I = V_1 I_1 = kV_1 \frac{V_C - V_2}{R} \]  \hspace{1cm} (2.30)

The transfer efficiency is

\[ \eta_{A1} = \frac{P_0}{P_I} = \frac{1-k}{k} \frac{V_2}{V_1} \frac{V_C - V_2}{V_C} = \frac{V_2}{V_1} \]  \hspace{1cm} (2.31)

From this equation it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of \( R, C, f, \) and \( k. \) If \( f = 5 \) kHz, \( V_1 = 21 \) V and \( V_2 = 14 \) V, and total \( C = 4000 \mu F, R = 50 \) m\( \Omega, \) for three \( k \) values the data are found in Table 2.6.

From the analysis and calculation, it can be seen that the conduction duty \( k \) does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds at \( k = 0.5. \)

### 2.3.1.2 Mode A2: Condition \( V_1 < V_2 \)

Mode A2, condition \( V_1 < V_2, \) is shown in Figure 2.6. Because two capacitors are connected in parallel during switch-on, the total capacitance \( C = 2 \times C_1 \)
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= 4000 μF. Input current \(i_1\) is two times that of capacitor current \(i_{c1}\). Two capacitors are connected in series during switch-off, the total capacitance \(C' = C_1/2 = 1000 \mu\text{F}\). Output current \(i_2\) is equal to capacitor current \(i_{c1}\). Suppose that the equivalent circuit resistance \(R = 50 \text{ m}\Omega\), \(V_1 = 14 \text{ V}\) and \(V_2 = 21 \text{ V}\), and the switching frequency is \(f = 5 \text{ kHz}\). The voltage and current across each capacitor are

\[
v_{c1}(t) = \begin{cases} 
  v_{c1}(0) + \frac{1}{C_1} \int_0^t i_{c1}(t)dt = v_{c1}(0) + \frac{t}{2C_1} \bar{i}_1 & \text{for } 0 \leq t < kT \\
  v_{c1}(kT) + \frac{1}{C_1} \int_{kT}^t i_{c1}(t)dt = v_{c1}(kT) - \frac{t - kT}{C_1} \bar{i}_2 & \text{for } kT \leq t < T 
\end{cases}
\]

(2.32)

\[
i_{c1}(t) = \begin{cases} 
  \frac{V_1 - v_{c1}(0)}{R}(1 - e^{-t/RC}) = \frac{V_1 - V_{c1}}{R} = \frac{\bar{i}_1}{2} & \text{for } 0 \leq t < kT \\
  -\frac{2v_{c1}(kT) - V_1}{R} e^{-t/RC} = -\frac{2V_{c1} - V_2}{R} = \bar{i}_2 & \text{for } kT \leq t < T 
\end{cases}
\]

(2.33)

Therefore,

\[
\bar{i}_1 = 2 \frac{1 - k}{k} \bar{i}_2
\]

(2.34)

Where \(\bar{i}_1\) is the average input current in the switch-on period \(kT\) that is equal to \(I_1/k\), and \(2 \bar{i}_2\) is the average output current in the switch-off period \((1 - k)T\) that is equal to \(I_2/(1 - k)\). Therefore, we have \(I_1 = 2I_2\). The variation of the voltage across capacitor \(C\) is

\[
\Delta v_c = \frac{1}{C} \int_0^{kT} i_c(t)dt = \frac{kT}{2C} \bar{i}_1 = \frac{k(V_1 - V_{c1})}{2fCR} & \text{for } 0 \leq t < kT
\]

or

\[
\Delta v_c = \frac{1}{C} \int_{kT}^{T} i_c(t)dt = \frac{(1 - k)T}{C} \bar{i}_2 = \frac{(1 - k)(2V_{c1} - V_2)}{fCR} & \text{for } kT \leq t < T
\]

To simplify the calculation, set \(k = 0.5\) we have:

\[
V_c = \frac{0.5V_1 + V_2}{2.5} = 11.2 \text{ V}
\]

(2.35)

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Hence

\[ \Delta v_c = \frac{k(V_1 - V_c)}{2fCR} = 0.7 \text{ V} \]  

(2.36)

We then have

\[ v_c(0) = V_c - \frac{\Delta v_c}{2} = 10.85 \text{ V} \]

and

\[ v_c(kT) = V_c + \frac{\Delta v_c}{2} = 11.55 \text{ V} \]

The average output current is

\[ I_2 = \frac{1}{T} \int_{kT}^{T} i_c(t)dt = (1-k) \frac{2V_c - V_2}{R} \]  

(2.37)

The average input current is

\[ I_1 = \frac{1}{T} \int_{0}^{kT} i_c(t)dt = k \frac{V_1 - V_c}{R} \]  

(2.38)

Output power is

\[ P_O = V_2I_2 = (1-k)V_2 \frac{2V_c - V_2}{R} \]  

(2.39)

Input power is

\[ P_I = V_1I_1 = kV_1 \frac{V_1 - V_c}{R} \]  

(2.40)

The transfer efficiency is

\[ \eta_{tr} = \frac{P_O}{P_I} = \frac{1-k}{k} \frac{V_1}{V_1 - V_c} \frac{V_2}{V_1 - V_c} = \frac{V_2}{2V_1} \]  

(2.41)
Switched Component Converters

From this equation it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of \( R, C, f, \) and \( k. \) If \( f = 5 \text{ kHz}, \) \( V_1 = 14 \text{ V} \) and \( V_2 = 21 \text{ V} \) and total \( C = 4000 \text{ mF}, R = 50 \text{ m}\Omega. \) For \( k = 0.5 \) the data are listed in Table 2.7.

From the analysis and calculation, it can be seen the power transfer efficiency only depends on the source and load voltages.

### 2.3.1.3 Experimental Results

A testing rig of two batteries 14 VDC and 21 VDC was prepared. The testing conditions were \( f = 5 \text{ kHz}, V_1 = 21 \text{ V} \) and \( V_2 = 14 \text{ V} \), total \( C = 4000 \text{ mF}, R = 50 \text{ m}\Omega. \) The experimental results for mode A are shown in Table 2.8. The equipment volume is 24 in\(^3\). The total average power density (PD) is 23.8 W/in\(^3\). This figure is much higher than the classical converters whose PD is usually less than 5 W/in\(^3\). Since the switching frequency is low, the electromagnetic interference (EMI) is weak.

### 2.3.2 Mode B (QII: Forward Regenerative Braking)

#### 2.3.2.1 Mode B1: Condition \( V_1 > V_2 \)

Mode B1, condition \( V_1 > V_2 \) is shown in Figure 2.7. This mode operation is similar to mode A2. Because two capacitors are connected in parallel during switch-on, the total capacitance \( C = 2 \times C_1 = 4000 \text{ mF}. \) Input current \( i_1 \) is two times the capacitor current \( i_{c1}. \) Two capacitors are connected in series during switch-off, the total capacitance \( C' = C_1/2 = 1000 \text{ mF}. \) Output current \( i_2 \) is equal to capacitor current \( i_{c1}. \) Suppose that the equivalent circuit resistance \( R = 50 \text{ m}\Omega, V_1 = 21 \text{ V} \) and \( V_2 = 14 \text{ V} \), and the switching frequency \( f = 5 \text{ kHz} \), in order to save the description we quote the results as follows. The voltage and current across each capacitor are

---

**TABLE 2.7**

<table>
<thead>
<tr>
<th>( k )</th>
<th>( V_c (\text{V}) )</th>
<th>( \Delta V_c (\text{V}) )</th>
<th>( I_1 (\text{A}) )</th>
<th>( I_2 (\text{A}) )</th>
<th>( P_1 (\text{W}) )</th>
<th>( P_o (\text{W}) )</th>
<th>( \eta_{A2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>11.2</td>
<td>0.7</td>
<td>28</td>
<td>14</td>
<td>392</td>
<td>294</td>
<td>0.75</td>
</tr>
</tbody>
</table>

**TABLE 2.8**

<table>
<thead>
<tr>
<th>( I_1 (\text{A}) )</th>
<th>( I_2 (\text{A}) )</th>
<th>( V_c (\text{V}) )</th>
<th>( P_I (\text{W}) )</th>
<th>( P_o (\text{W}) )</th>
<th>( h )</th>
<th>( P_D (\text{W/in}^3) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>33</td>
<td>32</td>
<td>17.5</td>
<td>693</td>
<td>448</td>
<td>0.646</td>
<td>571</td>
</tr>
</tbody>
</table>

---

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Therefore, 

\[ \bar{i}_2 = 2 \frac{1 - k}{k} \bar{i}_1 \]  

(2.44)

where \( \bar{i}_2 \) is the average input current in the switch-on period, \( kT \) is equal to \( I_1/k \), and \( 2 \bar{i}_1 \) is the average output current in the switch-off period \( (1 - k)T \) that is equal to \( I_1/(1 - k) \). Therefore, we have \( I_2 = 2I_1 \). The variation of the voltage across capacitor \( C \) is

\[
\Delta v_C = \frac{1}{C} \int_{0}^{kT} i_c(t) dt = \frac{kT}{2C} \bar{i}_2 = \frac{k(V_2 - V_{C1})}{2fCR} \\
0 \leq t \leq kT
\]
or

\[
\Delta v_C = \frac{1}{C} \int_{kT}^{T} i_c(t) dt = \frac{(1 - k)T}{C} \bar{i}_1 = \frac{(1 - k)(2V_C - V_t)}{2fCR} \\
kT \leq t \leq T
\]

To simplify the calculation, set \( k = 0.5 \):

\[ V_C = \frac{0.5V_t + V_0}{2.5} = 11.2 \text{ V} \]  

(2.45)

Hence

\[ \Delta v_C = \frac{k(V_2 - V_C)}{2fCR} = 0.7 \text{ V} \]  

(2.46)

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\[ v_c(0) = V_c - \frac{\Delta v_c}{2} = 10.85 \text{ V} \]

and

\[ v_c(kT) = V_c + \frac{\Delta v_c}{2} = 11.55 \text{ V} \]

The average output current is

\[ I_1 = \frac{1}{T} \int_{0}^{T} i_c(t)dt = (1-k)\frac{2V_c-V_1}{R} \quad (2.47) \]

The average input current is

\[ I_2 = \frac{1}{T} \int_{0}^{kT} i_c(t)dt = k\frac{V_2-V_c}{R} \quad (2.48) \]

Output power is

\[ P_o = V_1 I_1 = (1-k)V_1 \frac{2V_c-V_1}{R} \quad (2.49) \]

Input power is

\[ P_i = V_2 I_2 = kV_2 \frac{V_2-V_c}{R} \quad (2.50) \]

The transfer efficiency is

\[ \eta_{tr} = \frac{P_o}{P_i} = \frac{1-k \frac{V_1}{V_2}}{k \frac{V_2}{V_2-V_c} - \frac{V_1}{2V_2}} \quad (2.51) \]

From this equation it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of \( R \), \( C \), \( f \), and \( k \). If \( f = 5 \text{ kHz} \), \( V_1 = 21 \text{ V} \) and \( V_2 = 14 \text{ V} \) and total \( C = 4000 \mu\text{F} \), \( R = 50 \text{ m}\Omega \), for \( k = 0.5 \) the data are listed in Table 2.9.

From the analysis and calculation, it can be seen the power transfer efficiency only depends on the source and load voltages.

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2.3.2.2 Mode B2: Condition \( V_1 < V_2 \)

Mode B2, condition \( V_1 < V_2 \) is shown in Figure 2.8. This mode is similar to the mode A1. Because two capacitors are connected in parallel, the total capacitance \( C = C_1 + C_2 = 4000 \ \text{mF} \). Suppose that the equivalent circuit resistance \( R = 50 \ \text{m} \Omega \), \( V_2 = 21 \ \text{V} \) and \( V_1 = 14 \ \text{V} \), and the switching frequency \( f = 5 \ \text{kHz} \), the voltage and current across the capacitors are

\[
v_C(t) = \begin{cases} v_C(0) + \int_0^t i_C(t)dt & 0 \leq t < kT \\ v_C(kT) + \int_{kT}^T i_C(t)dt & kT \leq t < T \end{cases}
\]

(2.52)

\[
i_C(t) = \begin{cases} \frac{V_2 - v_C(0)}{R} (1 - e^{-t/RC}) = \frac{V_2 - V_C}{R} = \overline{I}_2 & 0 \leq t < kT \\ -\frac{v_C(kT) - V_1}{R} e^{-t/RC} = -\frac{V_C - V_1}{R} = -\overline{I}_1 & kT \leq t < T \end{cases}
\]

(2.53)

Therefore,

\[
\overline{I}_2 = \frac{1 - k}{k} \overline{I}_1
\]

(2.54)

Where \( \overline{I}_2 \) is the average input current in the switch-on period \( kT \) that is equal to \( I_2/k \), and \( \overline{I}_1 \) is the average output current in the switch-off period \( (1 - k)T \) that is equal to \( I_1/(1 - k) \). Therefore, we have \( I_2 = I_1 \). The variation of the voltage across capacitor \( C \) is

\[
\Delta v_C = \frac{1}{C} \int_0^{kT} i_C(t)dt = \frac{kT}{C} \overline{I}_2 = \frac{k(V_2 - V_C)}{fCR} & 0 \leq t < kT
\]

or

\[
\Delta v_C = \frac{1}{C} \int_{kT}^T i_C(t)dt = \frac{(1 - k)T}{C} \overline{I}_1 = \frac{(1 - k)(V_C - V_1)}{fCR} & kT \leq t < T
\]
Switched Component Converters

After calculation,

\[ V_c = kV_2 + (1 - k)V_1 \]  \hspace{1cm} (2.55)

Hence

\[ \Delta v_c = \frac{k(1 - k)(V_2 - V_1)}{fCR} \]  \hspace{1cm} (2.56)

We then have

\[ v_c(0) = V_c - \frac{\Delta v_c}{2} \]

and

\[ v_c(kT) = V_c + \frac{\Delta v_c}{2} \]

The average output current is

\[ I_1 = \frac{1}{T} \int_{kT}^{T} i_c(t)dt = (1 - k)\frac{V_c - V_1}{R} \]  \hspace{1cm} (2.57)

The average input current is

\[ I_2 = \frac{1}{T} \int_{0}^{kT} i_c(t)dt = k\frac{V_2 - V_c}{R} \]  \hspace{1cm} (2.58)

Output power is

\[ P_o = V_1I_1 = (1 - k)V_1\frac{V_c - V_1}{R} \]  \hspace{1cm} (2.59)

Input power is

\[ P_i = V_2I_2 = kV_2\frac{V_2 - V_c}{R} \]  \hspace{1cm} (2.60)

The transfer efficiency is
Advanced Multi-Quadrant Operation DC/DC Converters

The transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of $R$, $C$, $f$, and $k$. If $f = 5$ kHz, $V_2 = 21$ V and $V_1 = 14$ V and total $C = 4000$ µF, $R = 50$ mΩ. For three $k$ values we obtain the data in Table 2.10.

From the analysis and calculation, it can be seen that the conduction duty $k$ does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds at $k = 0.5$.

### 2.3.3 Mode C (QIII: Reverse Motoring)

This mode is similar to the mode A.

### 2.3.4 Mode D (QIV: Reverse Regenerative Braking)

This mode is similar to the mode B.

### 2.4 Switched Inductor Four-Quadrant DC/DC Luo-Converter

Although switched-capacitor DC/DC converters can reach high power density, their circuits are always very complex with difficult control. If the difference between input and output voltages is large, multiple switch-capacitor stages must be employed. Switched inductor DC/DC converters successfully overcome this disadvantage. Usually, only one inductor is required for each converter with 1-quadrant, 2-quadrant or 4-quadrant operation no matter how large the difference between the input and output voltages. Therefore, the switched inductor converter is a very simple circuit and consequently has high power density. This section introduces an SI four-quadrant DC/DC Luo-converter working in four-quadrant operation.

---

**TABLE 2.10**

The Calculation Results for Mode B2 ($V_1 < V_2$)

<table>
<thead>
<tr>
<th>$k$</th>
<th>$V_C$</th>
<th>$\Delta V_C$</th>
<th>$I_1$</th>
<th>$I_2$</th>
<th>$\eta_{A1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>16.8 V</td>
<td>1.68 V</td>
<td>33.6 A</td>
<td>33.6 A</td>
<td>0.67</td>
</tr>
<tr>
<td>0.5</td>
<td>17.5 V</td>
<td>1.75 V</td>
<td>35 A</td>
<td>35 A</td>
<td>0.67</td>
</tr>
<tr>
<td>0.6</td>
<td>18.2 V</td>
<td>1.68 V</td>
<td>33.6 A</td>
<td>33.6 A</td>
<td>0.67</td>
</tr>
</tbody>
</table>

\[
\eta_{B2} = \frac{P_D}{P_I} = \frac{1-k}{k} \frac{V_C - V_1}{V_2 - V_C} = \frac{V_1}{V_2} 
\]  

(2.61)
Switched Component Converters

This converter is shown in Figure 2.13a consisting of three switches, two diodes, and only one inductor \( L \). The source voltage \( V_1 \) and load voltage \( V_2 \) (e.g., a battery or DC motor back EMF) are usually constant voltages. \( R \) is the equivalent resistance of the circuit, it is usually small. Its equivalent circuits for quadrant I and II, and quadrant III and IV operation are shown in Figure 2.13b and c. Assuming the condition \( V_1 > |V_2| \), they are +42 V and ±14 V, respectively. Therefore, there are four quadrants (modes) of operation:

- **Mode A** (quadrant I: \( Q_I \)): the energy is transferred from source to positive voltage load
- **Mode B** (quadrant II: \( Q_{II} \)): the energy is transferred from positive voltage load to source
- **Mode C** (quadrant III: \( Q_{III} \)): the energy is transferred from source to negative voltage load
- **Mode D** (quadrant IV: \( Q_{IV} \)): the energy is transferred from negative voltage load to source

The first quadrant is called the forward motoring (Forw. Mot.) operation. \( V_1 \) and \( V_2 \) are positive, and \( I_1 \) and \( I_2 \) are positive as well. The second quadrant is called the forward regenerative (Forw. Reg.) braking operation. \( V_1 \) and \( V_2 \) are positive, and \( I_1 \) and \( I_2 \) are negative. The third quadrant is called the reverse motoring (Rev. Mot.) operation. \( V_1 \) and \( I_1 \) are positive, and \( V_2 \) and \( I_2 \) are negative. The fourth quadrant is called the reverse regenerative (Rev. Reg.) braking operation. \( V_1 \) and \( I_2 \) are positive, and \( I_1 \) and \( V_2 \) are negative. Each mode has two states: on and off. Usually, each state is operating in different conduction duty \( k \). The switching period is \( T \) where \( T = 1 / f \). The switch status is shown in Table 2.11.

Mode A operation is shown in Figure 2.14a (switch on) and b (switch off). During switch-on state, switch \( S_1 \) is closed. In this case the source voltage \( V_1 \) supplies the load \( V_2 \) and inductor \( L \), inductor current \( i_L \) increases. During switch-off state, diode \( D_2 \) is on. In this case current \( i_L \) flows through the load \( V_2 \) via the free-wheeling diode \( D_2 \), and it decreases.

Mode B operation is shown in Figure 2.15 a (switch on) and b (switch off). During switch-on state, switch \( S_2 \) is closed. In this case the load voltage \( V_2 \) supplies the inductor \( L \), inductor current \( i_L \) increases. During switch-off state, diode \( D_1 \) is on, current \( i_L \) flows through the source \( V_1 \) and load \( V_2 \) via the diode \( D_1 \), and it decreases.

Mode C operation is shown in Figure 2.16 a (switch on) and b (switch off). During switch-on state, switch \( S_1 \) is closed. The source voltage \( V_1 \) supplies the inductor \( L \), inductor current \( i_L \) increases. During switch-off state, diode \( D_2 \) is on. Current \( i_L \) flows through the load \( V_2 \) via the free-wheeling diode \( D_2 \), and it decreases.
Mode D operation is shown in Figure 2.17 a (switch on) and b (switch off). During switch-on state, switch $S_2$ is closed. The load voltage $V_2$ supplies the inductor $L$, inductor current $i_L$ increases. During switch-off state, diode $D_1$ is on. Current $i_L$ flows through the source $V_1$ via the diode $D_L$, and it decreases.

**FIGURE 2.13**
Four-quadrant switched-inductor DC/DC Luo-converters.

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TABLE 2.11
Switch Status

<table>
<thead>
<tr>
<th>Q No.</th>
<th>State</th>
<th>S₁</th>
<th>D₁</th>
<th>S₂</th>
<th>D₂</th>
<th>S₃</th>
<th>Source</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q₁, Mode A</td>
<td>on ON</td>
<td>ON1/2</td>
<td>V₁⁺</td>
<td>V₂⁺</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Forw. Mot.</td>
<td>off ON</td>
<td>ON1/2</td>
<td>I₁⁺</td>
<td>I₂⁺</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q₁, Mode B</td>
<td>on ON</td>
<td>ON1/2</td>
<td>V₁⁺</td>
<td>V₂⁺</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Forw. Reg.</td>
<td>off ON</td>
<td>ON1/2</td>
<td>I₁⁻</td>
<td>I₂⁻</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q₁, Mode C</td>
<td>on ON</td>
<td>ON3/4</td>
<td>V₁⁺</td>
<td>V₂⁻</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rev. Mot.</td>
<td>off ON</td>
<td>ON3/4</td>
<td>I₁⁺</td>
<td>I₂⁻</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q₁, Mode D</td>
<td>on ON</td>
<td>ON3/4</td>
<td>V₁⁺</td>
<td>V₂⁻</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rev. Reg.</td>
<td>off ON</td>
<td>ON3/4</td>
<td>I₁⁻</td>
<td>I₂⁺</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Omitted switches are off.

FIGURE 2.14
Mode A (quadrant I) operation.

FIGURE 2.15
Mode B (quadrant II) operation.

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2.4.1 Mode A (Q: Forward Motoring)

2.4.1.1 Continuous Mode

Refer to Figure 2.14a and suppose that $V_1 = +42$ V and $V_2 = +14$ V, $L = 0.3$ mH and the parasitic resistance $R = 3$ mΩ.

\[
\begin{align*}
V_1(t) & = \begin{cases} 
V_1 - V_2 - RL & 0 \leq t < kT \\
-(V_2 + RL) & kT \leq t < T 
\end{cases} \\
i_1(t) & = \begin{cases} 
i_1(0) + \left(\frac{V_1 - V_2}{L} - RL\right) t & 0 \leq t < kT \\
i_1(kT) - \frac{V_2 + RL}{L} (t - kT) & kT \leq t < T 
\end{cases}
\end{align*}
\]

(2.62)

(2.63)

where

\[
i_1(0) = I_i - \Delta i_i / 2
\]

(2.64)
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\[ i_L(kT) = I_L + \Delta i_L / 2 \] (2.65)

From Equations (2.62) and (2.63) the average inductor current is

\[ I_L = \frac{kV_1 - V_2}{R} \] (2.66)

The peak-to-peak variation of inductor current \( i_L \) is

\[ \Delta i_L = \frac{k(1-k)V_1}{fL} \] (2.67)

The variation ratio is

\[ \zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2} \cdot \frac{R}{2fL} \] (2.68)

Substituting Equations (2.66) and (2.67) into Equations (2.64) and (2.65), we have

\[ i_L(0) = \frac{kV_1 - V_2}{R} - \frac{k(1-k)V_1}{2fL} \] (2.69)

and

\[ i_L(kT) = \frac{kV_1 - V_2}{R} + \frac{k(1-k)V_1}{2fL} \] (2.70)

The average input current is

\[ I_1 = \frac{1}{T} \int_0^{kT} i_L(t)dt = k \frac{kV_1 - V_2}{R} \] (2.71)

The average output current is

\[ I_O = \frac{1}{T} \int_0^{T} i_L(t)dt = \frac{kV_1 - V_2}{R} \] (2.72)

Input power is

\[ P_1 = V_1 I_1 = kV_1 \frac{kV_1 - V_2}{R} \] (2.73)
Output power is

\[ P_0 = V_2 I_0 = V_2 \frac{kV_1 - V_2}{R} \]  \hspace{1cm} (2.74)

The transfer efficiency is

\[ \eta_A = \frac{P_0}{P_1} = \frac{V_2}{kV_1} \]  \hspace{1cm} (2.75)

The transfer efficiency only relies on conduction duty \( k \), the source and load voltages. It is independent of \( R, L, \) and \( f \).

If \( f = 1 \) kHz, \( L = 300 \) \( \mu \)H, \( R = 3 \) m\( \Omega \), \( k = 0.35 \), \( V_1 = 42 \) V and \( V_2 = 14 \) V, we find that

\[ I_L = 233 \text{ A, } \Delta i_L = 31.85 \text{ A } \zeta = 6.83\% \text{ I}_1 = 81.6 \text{ A, } I_0 = I_2 = 233 \text{ A,} \]

\[ P_0 = 32,672 \text{ W } P_1 = 3427 \text{ W } \eta_A = 95\% \]

**2.4.1.2 Discontinuous Mode**

From Equation (2.68), when \( \zeta \geq 1 \) the current \( i_L \) is discontinuous. The boundary between continuous and discontinuous regions is defined:

\[ \zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2} \frac{R}{2fL} \geq 1 \]

i.e.,

\[ \frac{k(1-k)V_1}{kV_1 - V_2} \frac{R}{2fL} \geq 1 \]

or

\[ k \leq \frac{V_2}{V_1} + k(1-k) \frac{R}{2fL} \]  \hspace{1cm} (2.76)

From Equation (2.76) the discontinuous conduction region is caused by the following factors:

- Switching frequency \( f \) is too low
- Duty cycle \( k \) is too small
• Inductance $L$ is too small
• Load resistor $R$ is too big

The whole conduction period is smaller than $T$. Assuming the conduction period is in the region between 0 and $t_1$ that is smaller than $T$. The filling coefficient $m_A$ is defined as

$$m_A = \frac{t_1 - kT}{(1 - k)T} \quad kT < t_1 \leq T \quad (2.77)$$

The voltage and current across inductor $L$ are

$$v_L(t) = \begin{cases} 
V_1 - V_2 - RL & 0 \leq t < kT \\
-(V_2 + RI_L) & kT \leq t < t_1 \\
0 & t_1 \leq t < T
\end{cases} \quad (2.78)$$

$$i_L(t) = \begin{cases} 
\frac{V_1 - V_2 - RL}{L}t & 0 \leq t < kT \\
\frac{V_1 kT - V_2 + RI_L}{L}t & kT \leq t < t_1 \\
0 & t_1 \leq t < T
\end{cases} \quad (2.79)$$

because

$$i_L(0) = 0$$

$$i_L(kT) = \frac{V_1 - V_2 - RL}{L} kT$$

$i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation $\Delta i_L$. From Equation (2.79) when $t = t_1$, $i_L(t_1) = 0$. Therefore, we have the following relation:

$$i_L(t_1) = \frac{V_1}{L} kT - \frac{V_2 + RI_L}{L} t_1 = 0$$

Therefore,

$$t_1 = \frac{V_1}{V_2 + RI_L} kT \quad (2.80)$$
Considering Equation (2.76),

\[ kT < t_1 < T \]

Since \( R \) is usually small, we can get

\[ t_1 = \frac{V_1}{V_2} kT \]

The average inductor current is

\[ I_L = \frac{1}{T} \int_{0}^{T} i_L(t)dt = \frac{1}{2T} i_L(kT) = \frac{V_1}{V_2 + RI_L} \frac{V_1 - V_2 - RI_L}{2fl} k^2 \]

Since \( R \) is usually small, it can be rewritten as

\[ I_L = \frac{V_1}{V_2} \frac{V_1 - V_2}{2fl} k^2 \]

The average input current is

\[ I_i = \frac{1}{T} \int_{0}^{T} i_i(t)dt = \frac{1}{2T} i_i(kT)kT = \frac{V_1 - V_2 - RI_L}{2fl} k^2 \]

The average output current is

\[ I_O = \frac{1}{T} \int_{0}^{T} i_O(t)dt = \frac{1}{2T} i_O(kT)t_1 = \frac{V_1 - V_2 - RI_L}{2fl} \frac{V_1}{V_2 + RI_L} k^2 \]

Input power is

\[ P_i = V_i I_i = V_1 \frac{V_1 - V_2 - RI_L}{2fl} k^2 \]

Output power is

\[ P_O = V_O I_O = V_2 \frac{V_1 - V_2 - RI_L}{2fl} \frac{V_1}{V_2 + RI_L} k^2 \]
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The transfer efficiency is

\[
\eta_{\text{A-dis}} = \frac{P_{i}}{P_{o}} = \frac{V_{2}}{V_{2} + RI_{L}} \quad (2.81)
\]

with

\[
k \leq \frac{V_{2}}{V_{1}} + k(1-k) \frac{R}{2fL}
\]

2.4.2 Mode B (QII: Forward Regenerative Braking)

2.4.2.1 Continuous Mode

Refer to Figure 2.15a, and suppose that \( V_{1} = +42 \text{ V} \) and \( V_{2} = +14 \text{ V} \), \( L = 0.3 \text{ mH} \) and the parasitic resistance \( R = 3 \text{ m}\Omega \).

\[
v_{i}(t) = \begin{cases} 
V_{2} - RI_{L} & 0 \leq t < kT \\
-(V_{1} - V_{2} + RI_{L}) & kT \leq t < T 
\end{cases}
\]

\[
i_{i}(t) = \begin{cases} 
i_{i}(0) + \frac{V_{2} - RI_{L}}{L} t & 0 \leq t < kT \\
i_{i}(kT) - \frac{V_{1} - V_{2} + RI_{L}}{L} (t - kT) & kT \leq t < T 
\end{cases}
\]

Where

\[
i_{i}(0) = I_{L} - \Delta i_{L} / 2 \quad (2.84)
\]

\[
i_{i}(kT) = I_{L} + \Delta i_{L} / 2 \quad (2.85)
\]

Since the inductor average voltage is zero, we have

\[k(V_{2} - RI_{L}) = (1-k)(V_{1} - V_{2} + RI_{L})\]

then:

\[
I_{L} = \frac{V_{2} - (1-k)V_{1}}{R} \quad (2.86)
\]

The peak-to-peak variation of inductor current \( i_{i} \) is
\[ \Delta i_L = \frac{k(1-k)V_1}{fL} \]  

(2.87)

The variation ratio is

\[ \zeta = \frac{\Delta i_L}{I_{k}} = \frac{k(1-k)V_1}{V_2-(1-k)V_1} \frac{R}{2fL} \]  

(2.88)

Substituting Equations (2.86) and (2.87) into Equations (2.84) and (2.85),

\[ i_L(0) = \frac{V_2-(1-k)V_1}{R} - \frac{k(1-k)V_1}{2fL} \]  

(2.89)

and

\[ i_L(kT) = \frac{V_2-(1-k)V_1}{R} + \frac{k(1-k)V_1}{2fL} \]  

(2.90)

The average input current is

\[ I_1 = \frac{1}{T} \int_{0}^{\tau} i_L(t)dt = \frac{V_2-(1-k)V_1}{R} \]  

(2.91)

The average output current is

\[ I_0 = \frac{1}{T} \int_{0}^{\tau} i_L(t)dt = (1-k) \frac{V_2-(1-k)V_1}{R} \]  

(2.92)

Input power is

\[ P_I = V_2I_1 = V_2 \frac{V_2-(1-k)V_1}{R} \]  

(2.93)

Output power is

\[ P_O = V_1I_0 = (1-k)V_1 \frac{V_2-(1-k)V_1}{R} \]  

(2.94)

The transfer efficiency is

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The transfer efficiency only relies on conduction duty $k$, the source and load voltages. It is independent of $R$, $L$, and $f$.

2.4.2.2 Discontinuous Mode

From Equation (2.88), when $\zeta \geq 1$ the current $i_L$ is discontinuous. The boundary between continuous and discontinuous regions is defined as:

$$\zeta = \frac{\Delta i_L}{I_L} = \frac{k(1-k)V_1}{V_2 - (1-k)V_1} \frac{R}{2fL} \geq 1$$

i.e.,

$$\frac{k(1-k)V_1}{V_2 - (1-k)V_1} \frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{1 - \frac{V_2}{V_1}}{1} + k(1-k) \frac{R}{2fL} \quad (2.96)$$

The whole conduction period is smaller than $T$. Assume that the conduction period is in the region between $0$ and $t_2$ that is smaller than $T$. The filling coefficient $m_B$ is defined as

$$m_B = \frac{t_2 - kT}{(1-k)T} \quad kT < t_2 \leq T \quad (2.97)$$

The voltage and current across inductor $L$ are

$$v_L(t) = \begin{cases} V_2 - R I_L & 0 \leq t < kT \\ -(V_1 - V_2 + R I_L) & kT \leq t < t_2 \\ 0 & t_2 \leq t < T \end{cases} \quad (2.98)$$

$$i_L(t) = \begin{cases} \frac{V_2 - R I_L}{L} t & 0 \leq t < kT \\ \frac{V_1}{L} kT - \frac{V_1 - V_2 + R I_L}{L} t & kT \leq t < t_2 \\ 0 & t_2 \leq t < T \end{cases} \quad (2.99)$$
because

\[ i_L(0) = 0 \]

\[ i_L(kT) = \frac{V_2 - R I_L}{L} kT \]

\( i_L(kT) \) is the peak value of inductor current \( i_L(t) \). It is also the peak-to-peak variation \( \Delta i_L \). From Equation (2.99) when \( t = t_2 \), \( i_L(t_2) = 0 \). Therefore, we have the following relation:

\[ i_L(t_2) = \frac{V_1}{L} kT - \frac{V_1 - V_2 + R I_L}{L} t_2 = 0 \]

Therefore,

\[ t_2 = \frac{V_1}{V_1 - V_2 + R I_L} kT \]

(2.100)

Considering Equation (2.86),

\[ kT < t_2 < T \]

Since \( R \) is usually small,

\[ t_2 = \frac{V_1}{V_1 - V_2} kT \]

The average inductor current is

\[ I_L = \frac{1}{T} \int_0^T i_L(t) dt = \frac{t_2}{2T} i_L(kT) = \frac{V_1}{V_1 - V_2 + R I_L} \frac{V_2 - R I_L}{2fL} k^2 \]

Since \( R \) is usually small, it can be rewritten as

\[ I_L = \frac{V_1}{V_1 - V_2} \frac{V_2}{2fL} k^2 \]

The average input current is

\[ I_i = \frac{1}{T} \int_0^T i_i(t) dt = \frac{i_i(kT)}{2T} t_2 = \frac{V_1}{V_1 - V_2 + R I_L} \frac{V_2 - R I_L}{2fL} k^2 \]
The average output current is

\[ I_O = \frac{1}{T} \int_{kT}^{(k+1)T} i_L(t) \, dt = \frac{1}{2T} (t_2 - kT) (V_2 - (RI_L)^2) k^2 \]

Input power is

\[ P_i = V_2 I_i = V_2 \frac{V_1}{V_1 - V_2 + RI_L} \frac{V_2 - RI_L}{k^2} \]

Output power is

\[ P_o = V_i I_o = V_1 \frac{V_2 - RI_L}{2fL} \frac{V_2 - RI_L}{V_1 - V_2 + RI_L} k^2 \]

The transfer efficiency is

\[ \eta_{\text{B-dis}} = \frac{P_o}{P_i} = \frac{V_2 - RI_L}{V_2} \] (2.101)

with

\[ k \leq (1 - \frac{V_2}{V_1}) + k(1 - k) \frac{R}{2fL} \]

### 2.4.3 Mode C (Q_{III}: Reverse Motoring)

#### 2.4.3.1 Continuous Mode

Refer to Figure 2.16a and suppose that \( V_1 = +42 \) V and \( V_2 = -14 \) V, \( L = 0.3 \) mH and the parasitic resistance \( R = 3 \) mΩ.

\[ v_L(t) = \begin{cases} V_1 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < T \end{cases} \] (2.102)

\[ i_L(t) = \begin{cases} i_L(0) + \frac{V_1 - RI_L}{L} t & 0 \leq t < kT \\ i_L(kT) - \frac{V_2 + RI_L}{L} (t - kT) & kT \leq t < T \end{cases} \] (2.103)

where

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\[ i_L(0) = I_L - \Delta i_L / 2 \]  
(2.104)

\[ i_L(kT) = I_L + \Delta i_L / 2 \]  
(2.105)

Since the inductor average voltage is zero,

\[ k(V_1 - RI_L) = (1 - k)(V_2 + RI_L) \]

\[ I_L = \frac{kV_1 - (1 - k)V_2}{R} \]  
(2.106)

The peak-to-peak variation of inductor current \( i_L \) is

\[ \Delta i_L = \frac{k(1 - k)(V_1 + V_2)}{fL} \]  
(2.107)

The variation ratio is

\[ \zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1 - k)(V_1 + V_2)}{kV_1 - (1 - k)V_2} \cdot \frac{R}{2fL} \]  
(2.108)

Substituting Equations (2.106) and (2.107) into Equations (2.104) and (2.105), we have

\[ i_L(0) = \frac{kV_1 - (1 - k)V_2 - k(1 - k)(V_1 + V_2)}{R} \cdot \frac{1}{2fL} \]  
(2.109)

and

\[ i_L(kT) = \frac{kV_1 - (1 - k)V_2 + k(1 - k)(V_1 + V_2)}{R} \cdot \frac{1}{2fL} \]  
(2.110)

The average input current is

\[ I_i = \frac{1}{T} \int_0^{kT} i_L(t)dt = k \frac{kV_1 - (1 - k)V_2}{R} \]  
(2.111)

The average output current is

\[ I_o = \frac{1}{T} \int_0^{kT} i_L(t)dt = (1 - k) \frac{kV_1 - (1 - k)V_2}{R} \]  
(2.112)
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Input power is

\[ P_I = V_I I_I = kV_1 \frac{kV_1 - (1-k)V_2}{R} \]  \hspace{1cm} (2.113)

Output power is

\[ P_O = V_2 I_O = (1-k)V_2 \frac{kV_1 - (1-k)V_2}{R} \]  \hspace{1cm} (2.114)

The transfer efficiency is

\[ \eta_c = \frac{P_O}{P_I} = \frac{(1-k)V_2}{kV_1} \]  \hspace{1cm} (2.115)

The transfer efficiency only relies on conduction duty \( k \), the source and load voltages. It is independent of \( R \), \( L \), and \( f \).

### 2.4.3.2 Discontinuous Mode

From Equation (2.108), when \( \zeta \geq 1 \) the current \( i_L \) is discontinuous. The boundary between continuous and discontinuous regions is defined:

\[ \zeta = \frac{\Delta i}{I_L} = \frac{k(1-k)(V_1 + V_2)}{kV_1 - (1-k)V_2} \frac{R}{2fL} \geq 1 \]

i.e.,

\[ \frac{k(1-k)(V_1 + V_2)}{kV_1 - (1-k)V_2} \frac{R}{2fL} \geq 1 \]

or

\[ k \leq \frac{V_2}{V_1 + V_2} + k(1-k) \frac{R}{2fL} \]  \hspace{1cm} (2.116)

The whole conduction period is smaller than \( T \). Assuming that the conduction period is in the region between 0 and \( t_s \). The filling coefficient \( m_c \) is defined as

\[ m_c = \frac{t_s - kT}{(1-k)f} \hspace{1cm} kT < t_s \leq T \]  \hspace{1cm} (2.117)
The voltage and current across inductor $L$ are

\[
v_L(t) = \begin{cases} 
  V_1 - R_1 I_L & 0 \leq t < kT \\
  -(V_2 + R_1 I_L) & kT \leq t < t_3 \\
  0 & t_3 \leq t < T 
\end{cases} \tag{2.118}
\]

\[
i_L(t) = \begin{cases} 
  \frac{V_1 - R_1}{L} t & 0 \leq t < kT \\
  \frac{V_1 + V_2}{L} - \frac{V_2 + R_1}{L} t & kT \leq t < t_3 \\
  0 & t_3 \leq t < T 
\end{cases} \tag{2.119}
\]

because

\[
i_L(0) = 0
\]

\[
i_L(kT) = \frac{V_1 - R_1}{L} kT
\]

$i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation $\Delta i_L$. From Equation (2.119) when $t = t_3$, $i_L(t_3) = 0$. Therefore, we have the following relation:

\[
i_L(t_3) = \frac{V_1 + V_2}{L} kT - \frac{V_2 + R_1}{L} t_3 = 0
\]

Therefore,

\[
t_3 = \frac{V_1 + V_2}{V_2 + R_1} kT \tag{2.120}
\]

Considering Equation (2.80),

\[kT < t_3 < T\]

Since $R$ is usually small,

\[
t_3 = \frac{V_1 + V_2}{V_2} kT
\]

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The average inductor current is

\[
I_L = \frac{1}{T} \int_0^{T} i_L(t) dt = \frac{1}{2T} i_L(kT) = \frac{V_1 + V_2}{V_2 + RI_L} \frac{V_1 - RI_L}{2fL} k^2
\]

Since \( R \) is usually small, it can be rewritten as

\[
I_L = \frac{V_1 + V_2}{V_2} \frac{V_1}{2fL} k^2
\]

The average input current is

\[
I_i = \frac{1}{T} \int_0^{T} i_i(t) dt = \frac{i_i(kT)}{2T} kT = \frac{V_i - RI_L}{2fL} k^2
\]

The average output current is

\[
I_o = \frac{1}{T} \int_0^{T} i_o(t) dt = \frac{i_o(kT)}{2T} (t_3 - kT) = \frac{(V_i - RI_L)^2}{2fL(V_2 + RI_L)} k^2
\]

Input power is

\[
P_I = V_I I_I = V_1 \frac{V_1 - RI_L}{2fL} k^2
\]

Output power is

\[
P_O = V_2 I_O = V_2 \frac{(V_i - RI_L)^2}{2fL(V_2 + RI_L)} k^2
\]

The transfer efficiency is

\[
\eta_{C-dis} = \frac{P_O}{P_I} = \frac{V_2}{V_1} \frac{V_1 - RI_L}{V_2 + RI_L}
\]

with

\[
k \leq \frac{V_2}{V_1 + V_2} + k(1-k) \frac{R}{2fL} \quad (2.121)
\]
2.4.4 Mode D (QIV: Reverse Regenerative Braking)

2.4.4.1 Continuous Mode

Refer to Figure 2.17a and suppose that $V_1 = +42 \, \text{V}$ and $V_2 = -14 \, \text{V}$, $L = 0.3 \, \text{mH}$ and the parasitic resistance $R = 3 \, \text{m\Omega}$.

\[
v_L(t) = \begin{cases} 
V_2 - RI_L & 0 \leq t < kT \\
-(V_1 + RI_L) & kT \leq t < T 
\end{cases} \tag{2.122}
\]

\[
i_L(t) = \begin{cases} 
i_L(0) + \frac{V_2 - RI_L}{L} t & 0 \leq t < kT \\
i_L(kT) - \frac{V_1 + RI_L}{L} (t - kT) & kT \leq t < T 
\end{cases} \tag{2.123}
\]

Where

\[
i_L(0) = I_L - \Delta i_L / 2 \tag{2.124}
\]

\[
i_L(kT) = I_L + \Delta i_L / 2 \tag{2.125}
\]

Since the inductor average voltage is zero we have

\[k(V_2 - RI_L) = (1-k)(V_1 + RI_L)\]

then:

\[I_L = \frac{kV_2 - (1-k)V_1}{R} \tag{2.126}\]

The peak-to-peak variation of inductor current $i_L$ is

\[\Delta i_L = \frac{k(1-k)(V_1 + V_2)}{fL} \tag{2.127}\]

The variation ratio is

\[\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)(V_1 + V_2)}{fL} \frac{R}{kV_2 - (1-k)V_1} \frac{1}{2fL} \tag{2.128}\]

Substituting Equations (2.126) and (2.127) into Equations (2.124) and (2.125),
and

\[
\begin{align*}
    i_L(kT) &= \frac{kV_2 - (1-k)V_1}{R} + \frac{k(1-k)(V_1 + V_2)}{2fL} \quad (2.130)
\end{align*}
\]

The average input current is

\[
I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt = k \cdot \frac{kV_2 - (1-k)V_1}{R} \quad (2.131)
\]

The average output current is

\[
I_O = \frac{1}{T} \int_{kT}^T i_L(t) dt = (1-k) \cdot \frac{kV_2 - (1-k)V_1}{R} \quad (2.132)
\]

Input power is

\[
P_I = V_2I_I = kV_2 \cdot \frac{kV_2 - (1-k)V_1}{R} \quad (2.133)
\]

Output power is

\[
P_O = V_1I_O = (1-k)V_1 \cdot \frac{kV_2 - (1-k)V_1}{R} \quad (2.134)
\]

The transfer efficiency is

\[
\eta_D = \frac{P_O}{P_I} = \frac{(1-k)V_1}{kV_2} \quad (2.135)
\]

The transfer efficiency only relies on conduction duty \( k \), the source and load voltages. It is independent of \( R, L, \) and \( f \).

### 2.4.4.2 Discontinuous Mode

From Equation (2.118), when \( \zeta \geq 1 \) the current \( i_L \) is discontinuous. The boundary between continuous and discontinuous regions is defined:
$\zeta = \frac{\Delta i_i}{I_i} = \frac{k(1-k)(V_1 + V_2)}{kV_2 - (1-k)V_i} \frac{R}{2fL} \geq 1$

i.e.,

$$\frac{k(1-k)(V_1 + V_2)}{kV_2 - (1-k)V_i} \frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_1}{V_1 + V_2} + k(1-k)\frac{R}{2fL}$$  (2.136)

The whole conduction period is smaller than $T$. Assuming that the conduction period is in the region between 0 and $t_4$, the filling coefficient $m_D$ is defined as

$$m_D = \frac{t_4 - kT}{(1-k)T} \quad kT < t_4 \leq T$$  (2.137)

The voltage and current across inductor $L$ are

$$v_i(t) = \begin{cases} 
V_2 - RI_i 
& 0 \leq t < kT \\
-(V_1 + RI_i) 
& kT \leq t < t_4 \\
0 
& t_4 \leq t < T 
\end{cases}$$  (2.138)

$$i_t(t) = \begin{cases} 
\frac{V_2 - RI_i}{L}t 
& 0 \leq t < kT \\
\frac{V_1 + V_2}{L}kT - \frac{V_1 + RI_i}{L}t 
& kT \leq t < t_4 \\
0 
& t_4 \leq t < T 
\end{cases}$$  (2.139)

because

$$i_t(0) = 0$$

$$i_t(kT) = \frac{V_2 - RI_i}{L}kT$$
\( i_L(kT) \) is the peak value of inductor current \( i_L(t) \). It is also the peak-to-peak variation \( \Delta i_L \). From Equation (2.139) when \( t = t_4 \), \( i_L(t_4) = 0 \). Therefore, we have the following relation:

\[
i_L(t_4) = \frac{V_1 + V_2}{2L} - \frac{V_1 + RI_L}{2L} t_4 = 0
\]

Therefore,

\[
t_4 = \frac{V_1 + V_2}{V_1 + RI_L} kT
\]

(2.140)

Considering Equation (2.136),

\[
kT < t_4 < T
\]

Since \( R \) is usually small, we can get

\[
t_4 = \frac{V_1 + V_2}{V_1} kT
\]

The average inductor current is

\[
I_L = \frac{1}{T} \int_0^{t_4} i_L(t)dt = \frac{t_4}{2T} i_L(kT) = \frac{V_1 + V_2}{V_1 + RI_L} \frac{V_2 - RI_L}{2fL} k^2
\]

Since \( R \) is usually small, it can be rewritten as

\[
I_L = \frac{V_1 + V_2}{V_1} \frac{V_2}{2fL} k^2
\]

The average input current is

\[
I_i = \frac{1}{T} \int_0^{t_4} i_i(t)dt = \frac{i_L(kT)}{2T} kT = \frac{V_2 - RI_L}{2fL} k^2
\]

The average output current is

\[
I_o = \frac{1}{T} \int_0^{t_4} i_o(t)dt = \frac{i_L(kT)}{2T} (t_4 - kT) = \frac{1}{2fL} \left( \frac{V_2 - RI_L}{V_1 + RI_L} \right)^2 k^2
\]
Input power is

\[ P_i = V_2 I_i = V_2 \frac{V_2 - RI_L}{2fL} k^2 \]

Output power is

\[ P_o = V_o I_o = V_1 \frac{1}{2fL} \frac{(V_2 - RI_L)^2}{V_1 + RI_L} \]

The transfer efficiency is

\[ \eta_{D-dis} = \frac{P_o}{P_i} = \frac{V_1 V_2 - RI_L}{V_2 V_1 + RI_L} \]

(2.141)

with

\[ k = \frac{V_1}{V_1 + V_2} + k(1-k) \frac{R}{2fL} \]

2.4.5 Experimental Results

A testing rig of a battery 14 VDC as a load and a source 42 VDC as the power supply was tested. The testing conditions were \( f = 1 \) to 5 kHz, \( V_{supply} = 42 \) V and \( V_i = -14 \) V, \( L = 0.3 \) mH, \( R = 3 \) mΩ, Volume = 2750(in³). The experimental results show that the total average PD is 28.8 W/in³. This figure is much higher than the classical converters whose PD is usually less than 5 W/in³. Since the switching frequency is low, the EMI is weak.
Bibliography

3

Positive Output Multiple-Lift Push-Pull
Switched-Capacitor Luo-Converters

The micro-power-consumption technique requires high power density DC/DC converters and power supply sources. The voltage lift technique is a popular application in electronic circuit design. Since the switched-capacitor can be integrated into the power integrated circuit (IC) chip, its size is small. Combining the switched-capacitor and voltage lift technique create a DC/DC converter with small size, high power density, high voltage transfer gain, high power efficiency, and low EMI.

3.1 Introduction

Switched-capacitor (SC) converters can perform in push-pull state with conduction duty cycle $k = 0.5$. This chapter introduces positive output multiple-lift push-pull switched-capacitor DC/DC Luo-converters. These converters can be sorted into several sub-series:

- Main series
- Additional series
- Enhanced series
- Re-enhanced series
- Multiple-enhanced series
Each circuit has one main switch $S$ and several slave switches as $S_i$ ($i = 1, 2, 3, \ldots n$). The number $n$ is called stage number. The main switch $S$ is on and slaves off during switch-on period $kT$, and $S$ is off and slaves on during switch-off period $(1-k)T$. The load is resistive load $R$. Input voltage and current are $V_{in}$ and $I_{in}$, output voltage and current are $V_O$ and $I_O$.

### FIGURE 3.1
Elementary circuit of P/O push-pull SC Luo-converter.

3.2 Main Series

The first three stages of the main series are shown in Figure 3.1 to Figure 3.3. For convenience they are called elementary circuit, re-lift circuit, and triple-lift circuit respectively, and are numbered as $n = 1, 2$ and 3.
3.2.1 Elementary Circuit

The elementary circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 3.1. Two switches $S$ and $S_1$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_O = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_O = 2V_{in}$$

(3.1)

Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_i$. The real output voltage is

$$V_O = 2V_{in} - \Delta V_i$$

(3.2)
3.2.2 Re-Lift Circuit

The re-lift circuit is derived from the elementary circuit by adding a parts-set: one slave switch, two switched-capacitors and three diodes \((S_2, C_3, C_4, D_3, D_4, D_5)\). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.2. The switches \(S\) and \((S_1, S_2)\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{i_n}\) and voltage across capacitor \(C_3\) is charged to \(V_1\) during switch-on. The voltage across capacitor \(C_2\) is charged to \(V_1 = 2V_{i_n} - \Delta V_1\) and voltage across capacitor \(C_4\) is charged to \(V_2 = 2V_1 - \Delta V_2\) during switch-off. Therefore, the output voltage is

\[
V_o = 2V_1 - \Delta V_2 = 4V_{i_n} - 2\Delta V_1 - \Delta V_2
\]  

(3.3)

where \(\Delta V_2\) is set for the same reason as \(\Delta V_1\).
3.2.3 Triple-Lift Circuit

The triple-lift circuit is derived from re-lift circuit by adding a parts-set: one more slave switch, two switched-capacitors and three diodes \((S_3-C_5-C_6-D_6-D_7-D_8)\). Its circuit diagram and equivalent circuits during switch-on and -off are shown in Figure 3.3. The switches \(S\) and \((S_1, S_2, S_3)\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{in}\), voltage across capacitor \(C_3\) is charged to \(v_1\) and voltage across capacitor \(C_5\) is charged to \(v_2\) during switch-on. The voltage across capacitor \(C_2\) is charged to \(V_1 = 2V_{in}\), voltage across capacitor \(C_4\) is charged to \(V_2 = 2V_1 - \Delta V_2\) and voltage across capacitor \(C_6\) is charged to \(V_O = 2V_2 - \Delta V_3\) during switch-off. Therefore, the output voltage is

\[
V_O = 2V_2 - \Delta V_3 = 4V_1 - 2\Delta V_2 - \Delta V_3 = 8V_{in} - 4\Delta V_1 - 2\Delta V_2 - \Delta V_3 \quad (3.4)
\]

where \(\Delta V_3\) is set as same reason as \(\Delta V_1\).

3.2.4 Higher Order Lift Circuit

The higher order lift circuit is designed by just multiple repeating of the parts mentioned in previous sections. The output voltage of the \(n^{th}\)-order lift circuit is

\[
V_O = 2^nV_{in} - \sum_{i=0}^{n-1} 2^i\Delta V_{n-i} \quad (3.5)
\]

3.3 Additional Series

The first three stages of the additional series are shown in Figure 3.4 to Figure 3.6. For convenience they are called elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit respectively, and are numbered as \(n = 1, 2,\) and \(3\).

3.3.1 Elementary Additional Circuit

The elementary additional circuit is derived from elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 3.4. Two switches \(S\) and \(S_1\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{in}\) during switch-on. The voltage across capacitors \(C_2\) and \(C_{11}\) is charged to \(V_1 = 2V_{in}\) during switch-off. Therefore, the output voltage is
Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$ and $\Delta V_O$ (for additional output parts). The real output voltage is

$$V_O = 3V_{in} - \Delta V_1 - \Delta V_O$$  \hspace{1cm} (3.7)

3.3.2 Re-Lift Additional Circuit

The re-lift additional circuit is derived from re-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.5. The switches $S$ and $(S_1, S_2)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$
is charged to $V_1$ and voltage across capacitor $C_{11}$ is charged to $V_2$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_3$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{12}$ is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 2V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O$$

(3.8)

where $\Delta V_2$ is set for the same reason as $\Delta V_1$.

### 3.3.3 Triple-Lift Additional Circuit

The triple-lift additional circuit is derived from triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off.
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FIGURE 3.6
Triple-lift additional circuit.
are shown in Figure 3.6. The switches $S$ and $(S_1, S_2, S_3)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$, voltage across capacitor $C_5$ is charged to $V_2$ and voltage across capacitor $C_{11}$ is charged to $V_3$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_6$ is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o$$  \hspace{1cm} (3.9)$$

where $\Delta V_3$ is set for the same reason as $\Delta V_1$.  

FIGURE 3.7
Re-lift enhanced circuit.
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FIGURE 3.8
Triple-lift enhanced circuit.

(a) Circuit diagram
(b) Equivalent circuit during switching-on (S on)
(c) Equivalent circuit during switching-off (S1, S2 and S3 on)
3.3.4 Higher Order Lift Additional Circuit

Higher order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. The output voltage of nth-lift additional circuit is

\[ V_{O-n} = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{in-i}) - \Delta V_n - \Delta V_O \]  

(3.10)

3.4 Enhanced Series

The first three stages of the enhanced series are shown in Figures 3.4, 3.7, and 3.8. For convenience they are called elementary enhanced circuit, re-lift enhanced circuit, and triple-lift enhanced circuit respectively, and are numbered as \( n = 1, 2, \) and 3.

3.4.1 Elementary Enhanced Circuit

The elementary enhanced circuit is derived from elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 3.4. The output voltage is

\[ V_O = V_1 + V_{in} = 3V_{in} \]  

(3.6)

Considering the voltage drops across the diodes and switches, we combine all values in a figure of \( \Delta V_1 \) and \( \Delta V_O \) (for additional output parts). The real output voltage is

\[ V_O = 3V_{in} - \Delta V_1 - \Delta V_O \]  

(3.7)

3.4.2 Re-Lift Enhanced Circuit

The re-lift enhanced circuit is derived from re-lift circuit by adding one DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.7. The switches \( S \) and \( (S_1, S_2) \) operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \), voltage across capacitor \( C_3 \) is charged to \( V_1 \) and voltage across capacitor \( C_{11} \) is charged to \( V_2 \) during switch-on. The voltage across capacitor \( C_2 \) is charged to \( V_1 = 2V_{in} - \Delta V \), voltage across capacitor \( C_4 \) is charged to \( V_2 = 2V_1 - \Delta V_2 \) and voltage across capacitor \( C_{12} \) is charged to \( V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O \) during switch-off. Therefore, the output voltage is

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\[ V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 9V_{in} - 6\Delta V_1 - 2\Delta V_2 - \Delta V_O \] (3.11)

where \( \Delta V_2 \) is set for the same reason as \( \Delta V_1 \).

### 3.4.3 Triple-Lift Enhanced Circuit

The triple-lift enhanced circuit is derived from re-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and -off are shown in Figure 3.8. The switches \( S_1, S_2, S_3 \) operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \), voltage across capacitor \( C_3 \) is charged to \( V_1 \), voltage across capacitor \( C_5 \) is charged to \( V_2 \) and voltage across capacitor \( C_{11} \) is charged to \( V_3 \) during switch-on. The voltage across capacitor \( C_4 \) is charged to \( V_1 = 2V_{in} - \Delta V_1 \), voltage across capacitor \( C_7 \) is charged to \( V_2 = 2V_1 - \Delta V_2 \) and voltage across capacitor \( C_6 \) is charged to \( V_3 = 2V_2 - \Delta V_3 \) during switch-off. Therefore, the output voltage is

\[ V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O = 27V_{in} - 18\Delta V_1 - 6\Delta V_2 - 2\Delta V_3 - \Delta V_O \] (3.12)

where \( \Delta V_3 \) is set for the same reason as \( \Delta V_1 \).

### 3.4.4 Higher Order Enhanced Lift Circuit

Higher order enhanced lift circuit is derived from the corresponding circuit of the main series circuit by adding the DEC in each stage circuit. The output voltage of the \( n \)th-order lift enhanced circuit is

\[ V_O = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}) - \Delta V_n - \Delta V_O \] (3.13)

### 3.5 Re-Enhanced Series

The first three stages of the re-enhanced series are shown in Figure 3.9 to Figure 3.11. For convenience they are called elementary re-enhanced circuit, re-lift re-enhanced circuit, and triple-lift re-enhanced circuit respectively, and are numbered as \( n = 1, 2, \) and 3.
3.5.1 Elementary Re-Enhanced Circuit

The elementary re-enhanced circuit is derived from elementary circuit by adding the DEC twice. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 3.9. Two switches S and S₁ operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \) during switch-on. The voltage across capacitors \( C_2 \) and \( C_{11} \) is charged to \( V_1 = 2V_{in} \) during switch-off. Therefore, the output voltage is

\[
V_O = V_1 + V_{in} = 4V_{in}
\]  

(3.14)
Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$ and $\Delta V_O$ (for additional output parts). The real output voltage is

$$V_O = 4V_{in} - \Delta V_1 - \Delta V_O$$  \hspace{1cm} (3.15)

### 3.5.2 Re-Lift Re-Enhanced Circuit

The re-lift re-enhanced circuit is derived from re-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.10. The switches S and ($S_1, S_2$) operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$, and voltage across capacitor $C_{11}$ is charged to $V_2$ during switch-on. The voltage across capacitor

---

**Figure 3.10**

Re-lift re-enhanced circuit.
FIGURE 3.11
Triple-lift re-enhanced circuit.
(a) Circuit diagram
(b) Equivalent circuit during switching-on (S on)
(c) Equivalent circuit during switching-off (S1, S2, and S3 on)
C_2 is charged to \( V_1 = 2V_{in} - \Delta V_1 \), voltage across capacitor \( C_4 \) is charged to \( V_2 = 2V_1 - \Delta V_2 \) and voltage across capacitor \( C_{12} \) is charged to \( V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O \) during switch-off. Therefore, the output voltage is

\[
V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (3.16)
\]

where \( \Delta V_2 \) is set for the same reason as \( \Delta V_1 \).

### 3.5.3 Triplet-Lift Re-enhanced Circuit

The triple-lift re-enhanced circuit is derived from triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.11. The switches \( S \) and \( (S_1, S_2, S_3) \) operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \), voltage across capacitor \( C_3 \) is charged to \( V_1 \), voltage across capacitor \( C_5 \) is charged to \( V_2 \) and voltage across capacitor \( C_{11} \) is charged to \( V_3 \) during switch-on. The voltage across capacitor \( C_2 \) is charged to \( V_1 = 2V_{in} - \Delta V_1 \), voltage across capacitor \( C_4 \) is charged to \( V_2 = 2V_1 - \Delta V_2 \) and voltage across capacitor \( C_6 \) is charged to \( V_3 = 2V_2 - \Delta V_3 \) during switch-off. Therefore, the output voltage is

\[
V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (3.17)
\]

where \( \Delta V_3 \) is set for the same reason as \( \Delta V_1 \).

### 3.5.4 Higher Order Lift Re-enhanced Circuit

Higher order lift re-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. The output voltage of the \( n \)th-lift re-enhanced circuit is

\[
V_O = (1.5 \times 2)^n V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} - \Delta V_m - \Delta V_O \quad (3.18)
\]

### 3.6 Multiple-enhanced Series

The first three stages of the multiple-enhanced series are shown in Figure 3.12 to Figure 3.14. For convenience they are called elementary multiple-enhanced circuit, re-lift multiple-enhanced circuit, and triple-lift multiple-enhanced circuit respectively, and are numbered as \( n = 1, 2, \) and \( 3 \).
3.6.1 Elementary Multiple-Enhanced Circuit

The elementary multiple-enhanced circuit is derived from elementary circuit by adding the DEC multiple ($j$) times. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 3.12. Two switches $S$ and $S_1$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$ during switch-on. The voltage across capacitors $C_2$ and $C_{11}$ is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$ V_O = V_1 + V_{in} = (1 + j)V_{in} \quad (3.19) $$
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FIGURE 3.13
Re-lift multiple-enhanced circuit.

(a) Circuit diagram
(b) Equivalent circuit during switching-on (S on)
(c) Equivalent circuit during switching-off (S1 and S2 on)

Re-lift multiple-enhanced circuit.
FIGURE 3.14
Triple-lift multiple-enhanced circuit.

(a) Circuit diagram
(b) Equivalent circuit during switching-on (S on)
(c) Equivalent circuit during switching-off (S, S2, and S3 on)
Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$ and $\Delta V_O$ (for additional output parts). The real output voltage is

$$V_O = (1 + j)V_{in} - \Delta V_1 - \Delta V_O$$  \hspace{1cm} (3.20)

### 3.6.2 Re-Lift Multiple-Enhanced Circuit

The re-lift multiple-enhanced circuit is derived from re-lift circuit by adding the DEC multiple ($j$) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.13. The switches $S$ and $(S_1, S_2)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$ and voltage across capacitor $C_{11}$ is charged to $V_2$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{12}$ is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O$$  \hspace{1cm} (3.21)

where $\Delta V_2$ is set for the same reason as $\Delta V_1$. 

---

**FIGURE 3.15**
The relationship among output current $I_o$, operation frequency $f$ and capacitance $C$. 

---
FIGURE 3.16
The family tree of multiple-lift push-pull switched-capacitor Luo-converters.

FIGURE 3.17
The simulation result of a triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.
3.6.3 Triple-Lift Multiple-Enhanced Circuit

The triple-lift multiple-enhanced circuit is derived from triple-lift circuit by adding the DEC multiple \((j)\) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.14. The switches \(S\) and \((S_1, S_2, S_3)\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{in}\), voltage across capacitor \(C_3\) is
charged to $V_1$, voltage across capacitor $C_3$ is charged to $V_2$ and voltage across capacitor $C_11$ is charged to $V_3$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_{4}$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{6}$ is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O$$  \hspace{1cm} (3.22)

where $\Delta V_3$ is set for the same reason as $\Delta V_1$.

### 3.6.4 Higher Order Lift Multiple-Enhanced Circuit

Higher order lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple ($j$) times in each stage circuit. The output voltage of the $n$th-lift multiple-enhanced circuit is

$$V_O = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}) - \Delta V_n - \Delta V_O$$  \hspace{1cm} (3.23)

### 3.7 Theoretical Analysis

The maximum output current is a key parameter of the DC-DC converter. The output voltage of DC-DC step-up converter can be shown as
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In Equation (3.24), \( m \) and \( n \) are the step-number of the converter and the number of the serial-parallel capacitors network respectively. \( T \) and \( k \) are the switch period and the duty-cycle ratio in the state 1, respectively. For the three-lift circuit, \( m = 1 \), \( n_1 = n_2 = 1 \) and \( f = 1/T \), we can write the Equation (3.24) as follows

\[
V_O = \frac{k_j V_{in} - k_j V_d}{1 + \sum_{i=1}^{m+1} \frac{n_i}{C_i} \left[ \frac{k T n_i}{R C_i} \right] \sum_{j=1}^{m+1} \frac{n_j^2}{n_j}}
\]

where \( k_s = \frac{\sum_{i=1}^{m+1} n_i}{\sum_{j=1}^{m+1} n_j} \) and \( k_d = \frac{\sum_{i=1}^{m+1} n_i(n_i + 1)}{m+1} \)

Since \( I_o = V_O/R \), we can write the output current of this three-lift circuit as follows

\[
I_o = \frac{3V_{in} - 4V_d - V_O}{1 - e^{-\frac{1}{2R C_2}} - e^{-\frac{1}{2R C_1}}} f
\]

where \( V_{in} \) is the source voltage assuming 10 V, \( V_O \) is the output voltage assuming 21.6 V, \( V_d \) is the voltage drop across diode, \( R \), which corresponds to the wire resistor of capacitor \( C \). In order to increase the output current of the converter, we selected Schottky barrier diode \( (V_d = 0.4 \text{ V}) \), then

\[
3V_{in} - 4V_d - V_O = 6.8 \text{ V}
\]

For getting the maximum output current, \( C_1 = C_2 = C \) have to be chosen. In addition we assumed \( R_1 = R_2 = R \). Therefore, the description of the output current can be simplified as

\[
I_o = 0.9 f C \left[ 1 - \exp\left(-1/2R/C\right) \right]
\]

Figure 3.15 shows the relationship among output current \( I_{O_{r}} \) operation frequency \( f \) and capacitance \( C \) on the basis of the equation. From the result, it is concluded that
1. Higher frequency can result in bigger output current, especially the capacitance of $C$ if the serial-parallel capacitors is not elevated for integration.

2. For a certain capacitor, there is a maximum frequency restriction, and it reduces when the capacitance is raised.

3. The output current can be up to 1A if the operation frequency $f$ of the converter and the capacitance $C$ of the serial-parallel capacitors are suitably chosen.

In addition, it can be shown from the equation deducing that the maximum ratio $P_o/C$ can be obtained by using the same capacitance of the serial-parallel capacitors in the structure. The theoretical analysis for the higher order lift circuits is similar to the above description.

### 3.8 Summary of This Technique

Using this technique, it is easy to design the Higher Order Lift circuit to obtain high output voltage. All these converters can be sorted in several sub-series: main series, additional series, enhanced series, re-enhanced series and multiple-enhanced series. The output voltage of the $n$th-lift circuit is

$$V_o = \begin{cases} 
2^n V_m - \sum_{i=0}^{m-1} 2^i \Delta V_{m-i} & \text{Main\_series} \\
1.5 \times (2^n V_m - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}) - \Delta V_m - \Delta V_o & \text{Additional\_series} \\
(3^n V_m - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}) - \Delta V_m - \Delta V_o & \text{Enhanced\_series} \\
(4^n V_m - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}) - \Delta V_m - \Delta V_o & \text{Re-Enhanced\_series} \\
[j + 2]^n V_m - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} - \Delta V_m - \Delta V_o & \text{Multiple-Enhanced\_series}
\end{cases}$$

(3.29)

From above formula, the family tree of positive output multiple-lift push-pull switched-capacitor Luo-converters is shown in Figure 3.16.

### 3.9 Simulation Results

To verify the design and calculation results, the PSpice simulation package was applied to these circuits. Choosing $V_i = 10 \text{ V}$, all capacitors $C_i = 2 \mu\text{F}$, $R$
= 60 k, k = 0.5 and f = 100 kHz, we obtain the current and voltage values in the following converters.

3.9.1 A Triple-Lift Circuit
Assume that the voltage drops $\Delta V_1$, $\Delta V_2$, and $\Delta V_3$ are about 4.2 V, the current waveforms of $I_{D2}$, $I_{DS}$, and $I_{D2S}$ then voltage values of $V_1$, $V_2$, and $V_O$ are 15.7 V, 27.2 V, and 50.7 V. The simulation results (current and voltage values) in Figure 3.17 are identically matched to the calculated results.

3.9.2 A Triple-Lift Additional Circuit
Assume that the voltage drops $\Delta V_1$, $\Delta V_2$, $\Delta V_3$, and $\Delta V_O$ are about 4.2 V, the current waveforms of $I_{D2}$, $I_{DS}$, $I_{D2S}$, and $I_{D12}$ then voltage values of $V_1$, $V_2$, $V_3$, and $V_O$ are 15.8 V, 27.5 V, 50.8 V, and 74.8 V. The simulation results (current and voltage values) shown in Figure 3.18 are identically matched to the calculated results.

3.10 Experimental Results
A test rig was constructed to verify the design and calculation results, and was compared with PSpice simulation results. With $V_i = 10$ V, all capacitors $C_i = 2 \mu F$, $R = 60$ k, $k = 0.5$ and $f = 100$ kHz, we measured the output voltage and the first diode current values in following converters.

3.10.1 A Triple-Lift Circuit
After careful measurement, we obtained the current waveform of $I_{D2}$ (shown in channel 1 with 5 A/Div in Figure 3.19) and voltage value of $V_O$ of 50.8 V (shown in channel 2 with 20 V/Div). The experimental results (current and voltage values) in Figure 3.17 are identically matched to the calculated and simulation results.

3.10.2 A Triple-Lift Additional Circuit
The experimental results (voltage and current values) are identically matching to the calculated and simulation results, as shown in Figure 3.20. The current waveform of $I_{D2}$ (shown in channel 1 with 5 A/Div) and voltage value of $V_O$ of 75 V (shown in channel 2 with 20 V/Div) have been obtained.
Bibliography


4

Negative Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters

Positive output multiple-lift push-pull switched-capacitor Luo-converters have been introduced in the previous chapter. Correspondingly, negative output multiple-lift push-pull switched-capacitor Luo-converters will be introduced in this chapter.

4.1 Introduction

Negative output multiple-lift push-pull switched-capacitor Luo-converters can be sorted into several sub-series:

- Main series
- Additional series
- Enhanced series
- Re-enhanced series
- Multiple-enhanced series

Each circuit has one main switch $S$ and several slave switches as $S_i \,(i = 1, 2, 3, \ldots n)$. The number $n$ is called stage number. The main switch $S$ is on and slaves off during switching-on period $kT$, and $S$ is off and slaves on during switch-off period $(1-k)T$. The load is resistive load $R$. Input voltage and current are $V_{in}$ and $I_{in}$, output voltage and current are $V_o$ and $I_o$.

Each circuit in the main series has one main switch $S$ and $n$ slave switches for $n$th stage circuit, $2n$ capacitors and $(3n - 1)$ diodes. Each circuit in the additional series has one main switch $S$ and $n$ slave switches for $n$th stage circuit, $2(n + 1)$ capacitors and $(3n + 1)$ diodes. Each circuit in the enhanced series has one main switch $S$ and $n$ slave switches for $n$th stage circuit, $4n$ capacitors and $(5n - 1)$ diodes. Each circuit in the re-enhanced series has one main switch $S$ and $n$ slave switches for $n$th stage circuit, $6n$ capacitors, and
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$(7n - 1)$ diodes. Each circuit in the multiple $(j$ times$)$-enhanced series has one main switch $S$ and $n$ slave switches for $n$th stage circuit, $2(1 + j)n$ capacitors and $[(3 + 2)n - 1]$ diodes. To simplify the calculation and explanation, all output values are the absolute values. The output voltage polarity is shown in the corresponding figure.

**4.2 Main Series**

The first three stages of the main series are shown in Figure 4.1 to Figure 4.3. For convenience they are called negative out-put (N/O) elementary circuit,
N/O re-lift push-pull SC circuit, and N/O triple-lift circuit respectively, and are numbered as \( n = 1, 2, \) and 3.

### 4.2.1 N/O Elementary Circuit

The elementary circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 4.1. Two switches \( S \) and \( S_1 \) operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \) during switch-on. The voltage across capacitor \( C_2 \) is charged to \( V_O = V_{in} \) during switch-off. Therefore, the output voltage is (absolute value):

\[
\text{FIGURE 4.2} \quad \text{N/O re-lift push-pull SC circuit.}
\]
Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$. The real output voltage is

$$V_o = V_{in} - \Delta V_1$$  \hfill (4.2)
4.2.2 N/O Re-Lift Circuit

The N/O re-lift circuit is derived from N/O elementary circuit by adding one slave switch, two switched-capacitors, and three diodes \((S_2-C_3-D_3-D_4)\). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.2. The switches \(S\) and \((S_1, S_2)\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{in}\) and voltage across capacitor \(C_2\) is charged to \(V_1\) during switch-on. The voltage across capacitor \(C_2\) is charged to \(V_1 = 2V_{in} - \Delta V_1\) and voltage across capacitor \(C_4\) is charged to \(V_0 = 2V_1 - \Delta V_2\) during switch-off. Therefore, the output voltage is

\[
V_0 = 2V_1 - \Delta V_2 - V_{in} = 3V_{in} - 2\Delta V_1 - \Delta V_2
\]  
(4.3)

where \(\Delta V_2\) is set for the same reason as \(\Delta V_1\).

4.2.3 N/O Triple-Lift Circuit

The N/O triple-lift circuit is derived from N/O re-lift circuit by adding one more slave switch, two switched-capacitors, and three diodes \((S_3-C_5-C_6-D_6-D_7)\). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.3. The switches \(S\) and \((S_1, S_2, S_3)\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{in}\), voltage across capacitor \(C_2\) is charged to \(V_1\) and voltage across capacitor \(C_3\) is charged to \(V_2\) during switch-on. The voltage across capacitor \(C_2\) is charged to \(V_1 = 2V_{in}\), voltage across capacitor \(C_4\) is charged to \(V_2 = 2V_1 - \Delta V_2\) and voltage across capacitor \(C_6\) is charged to \(V_0 = 2V_2 - \Delta V_3\) during switch-off. Therefore, the output voltage is

\[
V_0 = 2V_2 - \Delta V_3 - V_{in} = 4V_1 - 2\Delta V_2 - \Delta V_3 - V_{in}
\]

\[
= 7V_{in} - 4\Delta V_1 - 2\Delta V_2 - \Delta V_3
\]  
(4.4)

where \(\Delta V_3\) is set for the same reason as \(\Delta V_1\).

4.2.4 N/O Higher Order Lift Circuit

The N/O higher order lift circuit is can be designed by multiple repeating of the parts mentioned in previous sections. If the slave switches’ number is \(n\), the output voltage of the \(n\)th-lift circuit is

\[
V_0 = (2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-i}
\]  
(4.5)
4.3 Additional Series

The first three stages of the additional series are shown in Figure 4.4 to Figure 4.6. For convenience they are called N/O elementary additional circuit, N/O re-lift additional circuit, and N/O triple-lift additional circuit respectively, and are numbered as \( n = 1, 2, \) and 3.

FIGURE 4.4
N/O elementary additional/enhanced circuit.
4.3.1 N/O Elementary Additional Circuit

The N/O elementary additional circuit is derived from the N/O elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 4.4. Two switches $S$ and $S_1$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$ during switch-on. The voltage across capacitors $C_2$ and $C_{11}$ is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_O = V_1 + V_{in} - V_{in} = 2V_{in} \quad (4.6)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$ and $\Delta V_O$ (for additional output parts). The real output voltage is

$$V_O = 2V_{in} - \Delta V_1 - \Delta V_O \quad (4.7)$$

4.3.2 N/O Re-Lift Additional Circuit

The N/O re-lift additional circuit is derived from the N/O re-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.5. The switches $S$ and $(S_1, S_2)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$, and voltage across capacitor $C_{11}$ is charged to $V_2$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{12}$ is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = 5V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (4.8)$$

where $\Delta V_2$ is set for the same reason as $\Delta V_1$.

4.3.3 N/O Triple-Lift Additional Circuit

The N/O triple-lift additional circuit is derived from the N/O triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.6. The switches $S$ and $(S_1, S_2, S_3)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$, voltage across capacitor $C_5$ is charged to $V_2$, and voltage across capacitor $C_{11}$ is charged to $V_3$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across
capacitor \( C_6 \) is charged to \( V_3 = 2V_2 - \Delta V_3 \) during switch-off. Therefore, the output voltage is

\[
V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} = 11V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (4.9)
\]

where \( \Delta V_3 \) is set for the same reason as \( \Delta V_1 \).
4.3.4 N/O Higher Order Lift Additional Circuit

The N/O higher order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. The output voltage of the nth-lift circuit is

$$V_O = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{p-i}) - V_{in} - \Delta V_n - \Delta V_O \quad (4.10)$$
4.4 Enhanced Series

The first three stages of the enhanced series are shown in Figures 4.4, 4.7, and 4.8. For convenience, they are called N/O elementary enhanced circuit, N/O re-lift enhanced circuit, and N/O triple-lift enhanced circuit respectively, and are numbered as \( n = 1, 2, \) and 3.
4.4.1 N/O Elementary Enhanced Circuit

The N/O elementary enhanced circuit is derived from N/O elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 4.4. Therefore, the output voltage is

\[ V_O = V_1 + V_{in} - V_{in} = 2V_{in} \]  \hspace{1cm} (4.11)

Considering the voltage drops across the diodes and switches, we combine all values in a figure of \( \Delta V_1 \) and \( \Delta V_O \) (for additional output parts). The real output voltage is

\[ V_O = 2V_{in} - \Delta V_1 - \Delta V_O \]  \hspace{1cm} (4.12)

4.4.2 N/O Re-Lift Enhanced Circuit

The N/O re-lift enhanced circuit is derived from the N/O re-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.7. The switches \( S \) and \( (S_1, S_2) \) operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \), voltage across capacitor \( C_3 \) is charged to \( V_1 \), and voltage across capacitor \( C_{11} \) is charged to \( V_2 \) during switch-on. The voltage across capacitor \( C_2 \) is charged to \( V_1 = 2V_{in} - \Delta V_1 \), voltage across capacitor \( C_4 \) is charged to \( V_2 = 2V_1 - \Delta V_2 \), and voltage across capacitor \( C_{12} \) is charged to \( V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O \) during switch-off. Therefore, the output voltage is

\[ V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = 8V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \]  \hspace{1cm} (4.13)

where \( \Delta V_2 \) is set for the same reason as \( \Delta V_1 \).

4.4.3 N/O Triple-Lift Enhanced Circuit

The N/O triple-lift enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.8. The switches \( S \) and \( (S_1, S_2, S_3) \) operate in push-pull state. The voltage across capacitor \( C_1 \) is charged to \( V_{in} \), voltage across capacitor \( C_3 \) is charged to \( V_1 \), voltage across capacitor \( C_{11} \) is charged to \( V_2 \), and voltage across capacitor \( C_{12} \) is charged to \( V_3 \) during switch-on. The voltage across capacitor \( C_2 \) is charged to \( V_1 = 2V_{in} - \Delta V_1 \), voltage across capacitor \( C_4 \) is charged to \( V_2 = 2V_1 - \Delta V_2 \), and voltage across capacitor \( C_6 \) is charged to \( V_3 = 2V_2 - \Delta V_3 \) during switch-off. Therefore, the output voltage is
where $D_{V3}$ is set for the same reason as $D_{V1}$.

### 4.4.4 N/O Higher Order Lift Enhanced Circuit

The N/O higher order lift enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC in each stage circuit. The output voltage of the $n$th-lift circuit is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} = 26V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (4.14)$$

where $\Delta V_3$ is set for the same reason as $\Delta V_1$.

FIGURE 4.8
N/O triple-lift enhanced circuit.

$$V_O = [(3^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{in-i}] - \Delta V_{in} - \Delta V_O \quad (4.15)$$
4.5 Re-Enhanced Series

The first three stages of the re-enhanced series are shown in Figure 4.9 to Figure 4.11. For convenience, they are called N/O elementary re-enhanced circuit, N/O re-lift re-enhanced circuit, and N/O triple-lift re-enhanced circuit respectively, and are numbered as \( n = 1, 2, \) and 3.

4.5.1 N/O Elementary Re-Enhanced Circuit

The N/O elementary re-enhanced circuit is derived from N/O elementary circuit by adding the DEC twice. Its circuit diagram and its equivalent circuits...
during switch-on and switch-off are shown in Figure 4.9. Two switches $S$ and $S_1$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$ during switch-on. The voltage across capacitors $C_2$ and $C_{11}$ is charged to $V_1 = 2V_{in}$ during switch-off. The voltage across capacitors $C_{12}$ and $C_{13}$ is charged to $V_{C12} = 4V_{in}$ during switch-off. Therefore, the output voltage is

$$V_O = V_{C12} - V_{in} = 3V_{in}$$

(4.16)

Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$ and $\Delta V_O$ (for additional output parts). The real output voltage is

$$V_O = 3V_{in} - \Delta V_1 - \Delta V_O$$

(4.17)

4.5.2 N/O Re-Lift Re-Enhanced Circuit

The N/O re-lift re-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.10. The switches $S$ and $(S_1, S_2)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$ and voltage across capacitor $C_{11}$ is charged to $V_2$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{12}$ is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = 15V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O$$

(4.18)

where $\Delta V_2$ is set for the same reason as $\Delta V_1$.

4.5.3 N/O Triple-Lift Re-Enhanced Circuit

The N/O triple-lift re-enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.11. The switches $S$ and $(S_1, S_2, S_3)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$, voltage across capacitor $C_5$ is charged to $V_2$ and voltage across capacitor $C_{11}$ is charged to $V_3$ during switch-on. The voltage across capacitor $C_2$ is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{12}$ is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} = 63V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O$$

(4.19)
where $\Delta V_3$ is set for the same reason as $\Delta V_1$.

### 4.5.4 N/O Higher Order Lift Re-Enhanced Circuit

The N/O higher order lift re-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. The output voltage of the $n$th-lift circuit is

$$V_O = [(4^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}] - \Delta V_{n} - \Delta V_0 \quad (4.20)$$
FIGURE 4.11
N/O triple-lift re-enhanced circuit.
The first three stages of the multiple-enhanced series are shown in Figure 4.12 to Figure 4.14. For convenience they are called N/O elementary multiple-enhanced circuit, N/O re-lift multiple-enhanced circuit and N/O triple-lift multiple-enhanced circuit respectively, and are numbered as $n = 1, 2,$ and 3.

4.6 Multiple-Enhanced Series

The first three stages of the multiple-enhanced series are shown in Figure 4.12 to Figure 4.14. For convenience they are called N/O elementary multiple-enhanced circuit, N/O re-lift multiple-enhanced circuit and N/O triple-lift multiple-enhanced circuit respectively, and are numbered as $n = 1, 2,$ and 3.
4.6.1 N/O Elementary Multiple-Enhanced Circuit

The N/O elementary multiple-enhanced circuit is derived from the N/O elementary circuit by adding the DEC multiple \((j)\) times. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 4.12. Two switches \(S\) and \(S_1\) operate in push-pull state. The voltage across capacitor \(C_1\) is charged to \(V_{\text{in}}\) during switch-on. The voltage across capacitors \(C_2\) and \(C_{11}\) is charged to \(V_1 = 2V_{\text{in}}\) during switch-off. The voltage across capacitors \(C_{1(2j-1)}\) is charged to \(V_{C1(2j-1)} = (1 + j)V_{\text{in}}\) during switch-off. Therefore, the output voltage is

\[
V_O = V_{C1(2j-1)} - V_{\text{in}} = jV_{\text{in}} \tag{4.21}
\]
FIGURE 4.14
N/O triple-lift multiple-enhanced circuit.
Considering the voltage drops across the diodes and switches, we combine all values in a figure of $\Delta V_1$ and $\Delta V_O$ (for additional output parts). The real output voltage is

$$V_O = jV_{in} - \Delta V_1 - \Delta V_O$$  \hspace{1cm} (4.22)

### 4.6.2 N/O Re-Lift Multiple-Enhanced Circuit

The N/O re-lift multiple-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC multiple ($j$) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.13. The switches $S$ and $(S_1, S_2)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$ and voltage across capacitor $C_{11}$ is charged to $V_2$ during switch-on. The voltage across capacitor $C_2$ is charged to $V'_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_1$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_{12}$ is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = [(1 + j)^2 - 1]V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O$$  \hspace{1cm} (4.23)

where $\Delta V_2$ is set for the same reason as $\Delta V_1$.

### 4.6.3 N/O Triple-Lift Multiple-Enhanced Circuit

The N/O triple-lift multiple-enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC multiple ($j$) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.14. The switches $S$ and $(S_1, S_2, S_3)$ operate in push-pull state. The voltage across capacitor $C_1$ is charged to $V_{in}$, voltage across capacitor $C_3$ is charged to $V_1$, voltage across capacitor $C_5$ is charged to $V_2$ and voltage across capacitor $C_{11}$ is charged to $V_3$ during switch-on. The voltage across capacitor $C_2$ is charged to $V'_1 = 2V_{in} - \Delta V_1$, voltage across capacitor $C_4$ is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor $C_6$ is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in}$$

$$= [(1 + j)^3 - 1]V_{in} - 6\Delta V_1 - 3\Delta V_2 - 3\Delta V_3 - \Delta V_O$$  \hspace{1cm} (4.24)

where $\Delta V_3$ is set for the same reason as $\Delta V_1$. 

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4.6.4 N/O Higher Order Lift Multiple-Enhanced Circuit

The N/O higher order lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple \((j)\) times in each stage circuit. The output voltage of the \(n\)th order lift circuit is

\[
V_O = [(1 + j)^n - 1]V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O \tag{4.25}
\]

4.7 Summary of This Technique

Using this technique, it is easy to design N/O higher order lift circuits to obtain high output voltage. All these converters can be sorted in several subseries: main series, additional series, enhanced series, re-enhanced series, and multiple-enhanced series. The output voltage of the \(n\)th-lift circuit is

\[
V_O = 
\begin{cases} 
(2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} & \text{Main\_series} \\
(1.5 \times 2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Additional\_series} \\
(3^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Enhanced\_series} \\
(4^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Re-Enhanced\_series} \\
[(2 + j)^n - 1]V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Multiple-Enhanced\_series}
\end{cases}
\tag{4.26}
\]

From above formula, the family tree of negative output multiple-lift push-pull switched-capacitor Luo-converters is shown in Figure 4.15.

4.8 Simulation and Experimental Results

To verify the design and calculation results, PSpice simulation package was applied for these circuits. Choosing \(V_i = 10\) V, all capacitors \(C_i = 2\ \mu F\), \(R = 60\) k, \(k = 0.5\) and \(f = 100\) kHz, the voltage and current values are obtained from a N/O triple-lift circuit. The same conditions are applied to a test rig, experimental results are then obtained.

4.8.1 Simulation Results

Assume that the voltage drops \(\Delta V_1\), \(\Delta V_2\), and \(\Delta V_3\) are about 4.2 V, the voltage values of \(V_1\), \(V_2\), and \(V_3\) to be \(-5.2\) V, \(-16\) V, and \(-41\) V respectively and...
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FIGURE 4.15
The family tree of N/O multiple-lift push-pull switched-capacitor Luo-converters.

FIGURE 4.16
The simulation results of a N/O triple-lift circuit at condition \( k = 0.5 \) and \( f = 100 \text{ kHz} \).

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current waveforms of $I_{D2}$, $I_{DS}$, and $I_{DS}$ (the leak values are 103 A, 6.7 A, and 0.093 A respectively) are obtained. The simulation results voltage values in Figure 4.16 are identically matched to the calculated results.

4.8.2 Experimental Results

Assuming that the voltage drops $\Delta V_1$, $\Delta V_2$, and $\Delta V_3$ are still about 4.2 V, the output voltage $V_0$ (–41 V) and current waveform of $I_{D2}$ (leak value is 4.3 A) are obtained and shown in Figure 4.17, which are identically matched to the calculated and simulation results.

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Multiple-Quadrant Soft-Switch Converters

The third generation converters can transfer large amounts of power with high power density to actuators. However, its power losses are usually high during the transfer of large amounts of power since the power losses across the switch devices are high. The soft switch technique is an effective way to reduce the converter power losses and improve the efficiency. Therefore, it is a very popular method in industrial applications.

The fourth generation converters are called soft-switch converters. The soft-switch technique involves many methods implementing resonance characteristics. A popular method is the resonant-switch. Soft-switch converters are mainly implemented by the resonant technique. The resonant converters have drawn much attention in research applications. They are sorted into four categories:

- Load-resonant converters
- Resonant-DC-link converters
- High-frequency-link integral-half-cycle converters
- Resonant-switch converters

The converters of the first, second, and third categories can be applied in those cases depending on the load components and linking-cable. The converters of the fourth category are applied in the case depending on the resonant circuit in the switch-end, which are independent from load and link components. After about two decades of investigation and application, most industrial applications use resonant-switch converters.

Resonant-switch converters can perform in the over-resonant state, critical/optimum-resonant state, and quasi-resonant state. In order to determine two (current/voltage) zero-cross points for switch-on and switch-off, the quasi-resonant state is usually employed. The corresponding converter is called quasi-resonant converter (QRC). The quasi-resonant state can perform in full-waveform mode and half-waveform mode. The clue of soft switch technique focuses on the zero-cross point rather than the resonance. Consequently, there is no need in performing full-waveform mode. Most soft switch converters perform in half-waveform mode.
The zero-current-switch (ZCS) quasi-resonant-converters (QRC), zero-voltage-switch (ZVS) quasi-resonant-converters (QRC) and zero-transition (ZT) converters will be discussed in this chapter.

5.1 Introduction

Zero-current-switch quasi-resonant-converters implement ZCS operation. Since switches turn-on and turn-off at the moment that the current is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low. Therefore, the electromagnetic interference (EMI) is low, and electromagnetic susceptibility (EMS) and electromagnetic compatibility (EMC) are reasonable.

Zero-voltage-switch quasi-resonant-converters use the ZVS technique. Since switches turn-on and turn-off at the moment that the voltage is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low, so that the EMI is low, and EMS and EMC are reasonable.

ZCS-QRC and ZVS-QRC have large voltage and current stresses. In addition the conduction duty cycle $k$ and switch frequency $f$ are not individually adjusted. In order to overcome these drawbacks we designed zero-voltage-plus-zero-current-switches (ZV/ZCS) and zero-transition (ZT) converters, which implement the ZVS and ZCS technique. Since switches turn-on and -off at the moment that the voltage and/or current is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low, so that the EMI is low, and EMS and EMC are reasonable.

The ZCS technique significantly reduces the power losses across the switches during the switch-on and switch-off. Unfortunately, most papers discuss the converters only working at single quadrant operation. This paper introduces the multiple-quadrant DC/DC ZCS quasi-resonant Luo-converter. It performs the soft switch technique with a four-quadrant operation, which effectively reduces the power losses and largely increases the power transfer efficiency. The results obtained from analysis and design were compared and verified by practical test results.
5.2 Multiple-Quadrant DC/DC ZCS Quasi-Resonant Luo-Converters

A multiple-quadrant DC/DC ZCS quasi-resonant Luo-converter is shown in Figure 5.1. Circuit 1 implements the operation in quadrants I and II, i.e., two quadrant (I and II) 2CS quasi-resonant Luo-converters. Circuit 2 implements the operation in quadrants III and IV, i.e., two quadrant (III and IV) 2CS quasi-resonant Luo-converters. Circuit 1 and circuit 2 can be converted to each other by auxiliary changeover switch $S_a$. Auxiliary switch $S_a$ assists the two-quadrant operation in the same circuit. It is controlled by a logic quadrant-operation controller. Each circuit consists of one main inductor $L$ and two switches. Assuming that the main inductance $L$ is sufficient large,
the current $i_L$ remains constant. The source and load voltages are usually constant, e.g., $V_1 = 42$ V and $V_2 = \pm 28$ V. There are four modes of operation:

1. Mode A (quadrant I) : electrical energy is transferred from $V_1$ side to $V_2$ side.
2. Mode B (quadrant II): electrical energy is transferred from $V_2$ side to $V_1$ side.
3. Mode C (quadrant III) : electrical energy is transferred from $V_1$ side to $-V_2$ side.
4. Mode D (quadrant IV): electrical energy is transferred from $-V_2$ side to $V_1$ side.

Each mode has two states: on and off. The switch status of each state is shown in Table 5.1.

### 5.2.1 Mode A

Mode A is a ZCS buck converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 5.2. There are four time regions for the switch-on and -off period. The conduction duty cycle is $kT = (t_1 + t_2)$ when the input current flows through the switch $S_1$ and the main inductor $L$. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r1} - C_r$.

The natural resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_{r1}C_r}} \quad (5.1)$$

and the normalized impedance is

$$Z_1 = \frac{L_{r1}}{\sqrt{C_r}} \quad (5.2)$$

<table>
<thead>
<tr>
<th>Circuit // Switch or Diode</th>
<th>Mode A (Q-I)</th>
<th>Mode B (Q-II)</th>
<th>Mode C (Q-III)</th>
<th>Mode D (Q-IV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit</td>
<td>State-on</td>
<td>State-off</td>
<td>State-on</td>
<td>State-off</td>
</tr>
<tr>
<td>$S_1$</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>$D_1$</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>$S_2$</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>$S_a$</td>
<td>Position 1</td>
<td>Position 2</td>
<td>Position 3</td>
<td>Position 4</td>
</tr>
</tbody>
</table>

**Note:** The blank status means off.

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The resonant current (AC component) is
\[ i_{r}(t) = \frac{V_1}{Z_1} \sin(\omega_1 t + \alpha_1) \]  
\[ (5.3) \]

Considering the DC component \( I_L \), the peak current is
\[ i_{1\text{-peak}} = I_L + \frac{V_1}{Z_1} \]  
\[ (5.4) \]

5.2.1.1 Interval \( t = 0 \) to \( t_1 \)
Switch \( S_1 \) turns on at \( t = 0 \), the source current increases linearly with the slope \( V_1/L_{r1} \); this is called current linear rising interval. This current is smaller than the constant load current \( I_L \). Therefore, no current flows through the resonant capacitor \( C_r \).

When \( t = t_1 \), it is equal to \( I_L \). Therefore, the time is
\[ t_1 = \frac{I_L L_{r1}}{V_1} \]  
\[ (5.5) \]
And corresponding angular position is

\[ \alpha_1 = \sin^{-1}\left(\frac{I_1 Z_1}{V_1}\right) \]  

(5.6)

### 5.2.1.2 Interval \( t = t_1 \) to \( t_2 \)

In this period the current flows through the resonant capacitor \( C_r \). Circuit \( L_{r1} - C_r \) resonates; this is the resonance interval. The current waveform is a sinusoidal function. After its peak value, current descends down to \( I_L \), and then 0 if the converter works in subresonance state. Switch \( S_1 \) turns off at \( t = t_2 \). At this point we can see that the switch \( S_1 \) turns off at zero current condition. This period length is

\[ t_2 = \frac{1}{\omega_1} (\pi + \alpha_1) \]  

(5.7)

Simultaneously, the voltage across the capacitor \( C_r \) is a sinusoidal function as well. When \( t = t_2 \), the corresponding value \( v_{CO} \) of the capacitor voltage \( v_C \) is

\[ v_{CO} = V_1[1 + \sin(\pi / 2 + \alpha_1)] = V_1(1 + \cos \alpha_1) \]  

(5.8)

### 5.2.1.3 Interval \( t = t_2 \) to \( t_3 \)

Since the switch \( S_1 \) does not allow the resonant current to flow reversibly, the charge across the capacitor \( C_r \) will be discharged by the load current \( I_L \); this is the linear recovering interval. Because load current \( I_L \) is a constant current the voltage \( v_C \) decreases linearly from \( v_{CO} \) to 0 at \( t = t_3 \).

\[ t_3 = \frac{v_{CO} C_r}{I_L} \]  

(5.9)

### 5.2.1.4 Interval \( t = t_3 \) to \( t_4 \)

Capacitor voltage \( v_C \) cannot decrease to negative value because of the free-wheeling diode \( D_2 \); this is the normal off interval. The load current commutates from \( C_r \) to \( D_2 \) at \( t = t_3 \). Since then, the load current free-wheels through the main inductor \( L \), load voltage source \( V_2 \) and free-wheeling diode \( D_2 \). The time length \( t_4 \) of this period depends on the design requirement. Ignoring the power losses and \( I_2 = I_L \), we have the input average current \( I_1 \):

\[ I_1 = \frac{I_1 V_2}{V_1} = \frac{t_1 + t_2}{T} \left( I_L + \frac{V_1}{Z_1} \cos \alpha_1 \right) \]  

(5.10)

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Therefore,

\[ t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_L} (I_L + \frac{V_1}{Z_1} \cos \frac{1}{2} (t_1 + t_2 + t_3 + t_4) ) \quad (5.11) \]

We have the conduction duty

\[ k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \quad (5.12) \]

The whole repeating period is

\[ T = t_1 + t_2 + t_3 + t_4 \quad (5.13) \]

And corresponding frequency is

\[ f = \frac{1}{T} \quad (5.14) \]

5.2.2 Mode B

Mode B is a ZCS boost converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.3. There are four time regions for the switch-on and -off period. The conduction duty cycle is \( kT = (t_1 + t_2) \), but the output current only flows through the source \( V_1 \) in the period \( t_1 \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_{r2} - C_r \).

The resonance frequency is

\[ \omega_2 = \frac{1}{\sqrt{L_{r2} C_r}} \quad (5.15) \]

and the normalized impedance is

\[ Z_2 = \sqrt{\frac{L_{r2}}{C_r}} \quad (5.16) \]

The resonant current (AC component) is

\[ i_r(t) = \frac{V_1}{Z_2} \sin(\omega_2 t + \alpha_2) \quad (5.17) \]
Considering the DC component $I_L$, the peak current is

$$i_{2\text{-peak}} = I_L + \frac{V_1}{Z_2} \quad (5.18)$$

### 5.2.2.1 Interval $t = 0$ to $t_1$

Switch $S_2$ turns on at $t = 0$, the voltage across capacitor $C_r$ is equal to $V_1$. The inductor current $i_{L,2}$ increases linearly with the slope $V_1/L_{r1}$. This current is smaller than the constant load current $I_L$. Therefore, no current flows through the resonant capacitor $C_r$.

When $t = t_1$, it is equal to $I_L$. Therefore, the time is

$$t_1 = \frac{I_L L_{r2}}{V_1} \quad (5.19)$$

and corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{I_L Z_2}{V_1}\right) \quad (5.20)$$
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5.2.2.2 Interval \( t = t_1 \) to \( t_2 \)

In this period the current flows through the resonant capacitor \( C_r \). Circuit \( L_r - C_r \) resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to \( I_r \) and then 0 if the converter works in subresonance state. Switch \( S_2 \) turns off at \( t = t_2 \).

At this point we can see that the switch \( S_2 \) turns off at zero current condition. This period length is

\[
t_2 = \frac{1}{\omega_2} (\pi + \alpha_2)
\]

Simultaneously, the voltage across the capacitor \( C_r \) is a sinusoidal function as well. When \( t = t_2 \), the corresponding value \( v_{CO} \) of the capacitor voltage \( v_c \) is

\[
v_{CO} = -V_1 \sin(\pi/2 + \alpha_2) = -V_1 \cos \alpha_2
\]

5.2.2.3 Interval \( t = t_2 \) to \( t_3 \)

Since the switch \( S_2 \) does not allow the resonant current to flow reversibly, the charge across the capacitor \( C_r \) will be discharged by the load current \( I_L \).

Because load current \( I_L \) is a constant current the voltage \( v_c \) increases linearly from \( v_{CO} \) to \( V_1 \) at \( t = t_3 \),

\[
t_3 = \frac{(V_1 - v_{CO})C_r}{I_L}
\]

5.2.2.4 Interval \( t = t_3 \) to \( t_4 \)

Capacitor voltage \( v_c \) cannot be higher than \( V_1 \) because of the diode \( D_1 \). The main inductor current commutes from \( C_r \) to \( D_1 \) at \( t = t_3 \). Since then, the load current flows through the main inductor \( L \), diode \( D_1 \), source voltage \( V_1 \) and load voltage \( V_2 \). The time length \( t_4 \) of this period depends on the design requirement. Ignoring the power losses and \( I_2 = I_L \), we have the output average current \( I_1 \):

\[
I_1 = \frac{I_1 V_2}{V_1} = \frac{t_4}{T} I_L
\]

or

\[
\frac{V_2}{V_1} = \frac{t_4}{T} = \frac{t_4}{t_1 + t_2 + t_3 + t_4}
\]

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Therefore,

\[ t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1} \]  
(5.26)

We have the conduction duty

\[ k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \]  
(5.27)

The whole repeating period is

\[ T = t_1 + t_2 + t_3 + t_4 \]  
(5.28)

and corresponding frequency is

\[ f = 1 / T \]  
(5.29)

5.2.3 Mode C

Mode C is a ZCS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.4. There are four time regions for the switch-on and -off period. The conduction duty cycle is \( kT = (t_1 + t_2) \) when the input current flows through the switch \( S_1 \) and the main inductor \( L \). The output current only flows through \( V_2 \) in \( t_4 \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_{r1} - C_r \).

The resonance frequency is

\[ \omega_1 = \frac{1}{\sqrt{L_{r1}C_r}} \]  
(5.30)

and the normalized impedance is

\[ Z_1 = \frac{L_{r1}}{\sqrt{C_r}} \]  
(5.31)

The resonant current (AC component) is

\[ i_r(t) = \frac{V}{Z_1} \sin(\omega_1 t + \alpha_1) \]  
(5.32)
Considering the DC component $I_L$, the peak current is

\[ i_{1,\text{peak}} = I_L + \frac{V_1}{Z_1} \quad (5.33) \]

5.2.3.1 Interval $t = 0$ to $t_1$

Switch $S_1$ turns on at $t = 0$, the voltage across capacitor $C_r$ is equal to $V_2$. The inductor current $i_{L1}$ increases linearly with the slope $(V_1 + V_2)/L_{r1}$. This current is smaller than the constant load current $I_L$. Therefore, no current flows through the resonant capacitor $C_r$.

When $t = t_1$, it is equal to $I_L$. Therefore, the time

\[ t_1 = \frac{I_L L_{r1}}{V_1 + V_2} \quad (5.34) \]

and corresponding angular position is

\[ \alpha_1 = \sin^{-1}\left(\frac{I_L Z_{r1}}{V_1}\right) \quad (5.35) \]
Before $S_1$ turns on at $t = 0$, free-wheeling diode $D_2$ is conducted. Therefore the capacitor voltage $v_c$ across the resonant capacitor $C_r$ is equal to $V_2$ in this interval.

**5.2.3.2 Interval $t = t_1$ to $t_2$**

In this period the current flows through the resonant capacitor $C_r$. Circuit $L_1 - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to $I_L$ and then 0 if the converter works in subresonance state. Switch $S_1$ turns off at $t = t_2$.

At this point we can see that the switch $S_1$ turns off at zero current condition. This period length is

$$t_2 = \frac{1}{\omega_1} (\pi + \alpha_i)$$

(5.36)

Simultaneously, the voltage across the capacitor $C_r$ is a sinusoidal function as well. The resonant amplitude is equal to $V_1$. When $t = t_2$, the corresponding value $v_{CO}$ of the capacitor voltage $v_c$ is

$$v_{CO} = V_1 - V_2 + V_1 \sin(\pi / 2 + \alpha_i) = V_1(1 + \cos \alpha_i) - V_2$$

(5.37)

**5.2.3.3 Interval $t = t_2$ to $t_3$**

Since the switch $S_1$ does not allow the resonant current to flow reversibly, the charge across the capacitor $C_r$ will be discharged by the load current $I_L$. Because load current $I_L$ is a constant current the voltage $v_c$ decreases linearly from $v_{CO}$ to $-|V_2|$ at $t = t_3$. In this interval, the free-wheeling diode $D_2$ does not conduct because it is reversibly biased.

$$t_3 = \frac{(v_{CO} + V_2)C_r}{I_L}$$

(5.38)

**5.2.3.4 Interval $t = t_3$ to $t_4$**

Capacitor voltage $v_c$ is equal to $V_2$ at $t = t_3$, the free-wheeling diode $D_2$ then conducted. The main inductor current commutates from $C_r$ to $V_2$ at $t = t_3$. Since then, the load current free-wheels through the main inductor $L$, load voltage source $V_2$ and free-wheeling diode $D_2$. The time length $t_4$ of this period depends on the design requirement. Ignoring the power losses, we have the input average current $I_1$:

$$I_1 = \frac{t_3 + t_2}{T}(I_1 + \frac{V_1}{Z_L} \cos \frac{\pi}{2 + \alpha_i})$$

(5.39)
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and

\[ I_2 = \frac{t_4}{T} I_L \]  

(5.40)

Therefore,

\[ t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_L} (I_L + \frac{V_1}{Z_1} \cos \frac{1}{2} - \frac{1}{2}) \]  

(5.41)

We have the conduction duty

\[ k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \]  

(5.42)

The whole repeating period is

\[ T = t_1 + t_2 + t_3 + t_4 \]  

(5.43)

and corresponding frequency is

\[ f = \frac{1}{T} \]  

(5.44)

5.2.4 Mode D

Mode D is a ZCS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.5. There are four time regions for the switch-on and -off period. The conduction duty cycle is \( kT = (t_1 + t_3) \), but the output current only flows through the source \( V_1 \) in the period \( t_4 \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_{2r} - C_r \).

The resonance frequency is

\[ \omega_2 = \frac{1}{\sqrt{L_{2r}C_r}} \]  

(5.45)

and the normalized impedance is

\[ Z_2 = \frac{L_{2r}}{C_r} \]  

(5.46)
The resonant current (AC component) is

\[ i_{r}(t) = \frac{V_1}{Z_2} \sin(\omega t + \alpha) \] (5.47)

Considering the DC component \( I_L \), the peak current is

\[ i_{2-peak} = I_L + \frac{V_1}{Z_2} \] (5.48)

**5.2.4.1 Interval \( t = 0 \ to \ t_1 \)**

Switch \( S_2 \) turns on at \( t = 0 \), the voltage across capacitor \( C_r \) is equal to \( V_1 \). The inductor current \( i_{L2} \) increases linearly with the slope \((V_1 + V_2)/L_{r2}\). This current is smaller than the constant load current \( I_L \). Therefore, no current flows through the resonant capacitor \( C_r \).

When \( t = t_1 \), it is equal to \( I_L \). Therefore, the time

\[ t_1 = \frac{I_L L_{r2}}{V_1 + V_2} \] (5.49)
and corresponding angular position is

\[ \alpha_2 = \sin^{-1}\left(\frac{I_1 Z_2}{V_2}\right) \]  

(5.50)

5.2.4.2 Interval \( t = t_1 \) to \( t_2 \)

In this period the current flows through the resonant capacitor \( C_r \). Circuit \( L_{r2} - C_r \) resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to \( I_L \), and then 0 if the converter works in subresonance state. Switch \( S_2 \) turns off at \( t = t_2 \).

At this point we can see that the switch \( S_2 \) turns off at zero current condition. This period length is

\[ t_2 = \frac{1}{\omega_2} (\pi + \alpha_2) \]  

(5.51)

Simultaneously, the voltage across the capacitor \( C_r \) is a sinusoidal function as well. When \( t = t_2 \), the corresponding value \( v_{CO} \) of the capacitor voltage \( v_C \) is

\[ v_{CO} = (V_1 - V_2) - V_2 \sin(\pi / 2 + \alpha_2) = V_1 - V_2 (1 + \cos \alpha_2) \]  

(5.52)

5.2.4.3 Interval \( t = t_2 \) to \( t_3 \)

Since the switch \( S_2 \) does not allow the resonant current to flow reversibly, the charge across the capacitor \( C_r \) will be discharged by the load current \( I_L \).

Because load current \( I_L \) is a constant current the voltage \( v_C \) increases linearly from \( v_{CO} \) to \( V_1 \) at \( t = t_3 \),

\[ t_3 = \frac{(V_1 - v_{CO}) C_r}{I_L} = \frac{V_1 C_r}{I_L} (1 + \cos \alpha_2) \]  

(5.53)

5.2.4.4 Interval \( t = t_3 \) to \( t_4 \)

Capacitor voltage \( v_C \) cannot be higher than \( V_1 \) because of the diode \( D_1 \) conducted. The main inductor current commutates from \( C_r \) to \( D_1 \) at \( t = t_3 \). Since then, the output current \( I_1 \) flows through the main inductor \( L \), diode \( D_1 \) source voltage \( V_1 \) and load voltage \( V_2 \). The time length \( t_4 \) of this period depends on the design requirement. Ignoring the power losses, we have the output average current \( I_1 \):

\[ I_1 = \frac{I_1 V_2}{V_1} = \frac{t_4}{T} I_L \]  

(5.54)
and

\[ I_2 = \frac{t_1 + t_2}{T} \left( I_L + \frac{V_2}{Z_L} \cos \frac{\pi t}{2 + \cos \frac{\pi}{2}} \right) \]  \hspace{1cm} (5.55)

Therefore,

\[ t_4 = \frac{V_2 (t_1 + t_2)}{V_L I_L} \left( I_L + \frac{V_2}{Z_L} \cos \frac{\pi t}{2 + \cos \frac{\pi}{2}} \right) \] \hspace{1cm} (5.56)

We have the conduction duty

\[ k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \] \hspace{1cm} (5.57)

The whole repeating period is

\[ T = t_1 + t_2 + t_3 + t_4 \] \hspace{1cm} (5.58)

And corresponding frequency is

\[ f = \frac{1}{T} \] \hspace{1cm} (5.59)

5.2.5 Experimental Results

A testing rig with a battery of ±28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are: \( V_1 = 42 \text{ V} \) and \( V_2 = ±28 \text{ V}, L = 30 \mu\text{H}, L_{r1} = L_{r2} = 1 \mu\text{H}, C_r = 4 \mu\text{F} \) and the volume is 40 in\(^3\). The experimental results are shown in Table 5.2. The average power transfer efficiency is 96.3\%, and the total average power density (PD) is 17.1 W/in\(^3\). This figure is much higher than the classical converters whose PD is usually less than 5 W/in\(^3\). Since the switch frequency is low (\( f < 41 \text{ kHz} \)) and this converter works at the mono-resonance frequency, the components of the high-order harmonics are small. Applying FFT analysis, the total harmonic distortion (THD) is very small, thus the EMI is weak, and the EMS and EMC are reasonable.

5.3 Multiple-Quadrant DC/DC ZVS Quasi Resonant Luo-Converter

Many industrial applications require the multi-quadrant operation with ZVS technique, since it significantly reduces the power losses. Unfortunately,
most of the papers discuss the ZVS converters only working at single quadrant operation. Four-quadrant DC/DC ZCS quasi-resonant Luo-converter effectively reduces the power losses and largely increases the power transfer efficiency. This is shown in Figure 5.6. Circuit 1 implements the operation in quadrants I and II, circuit 2 implements the operation in quadrants III and IV. Circuit 1 and circuit 2 can be converted to each other by an auxiliary change-over switch $S_3$, which is illustrated in circuit 3. Each circuit consists of one main inductor $L$ and two switches. Assuming that the main inductance $L$ is sufficient large, the current $i_L$ is constant. The source and load voltages are usually constant, e.g., $V_1 = 42$ V and $V_2 = \pm 28$ V. There are four modes of operation:

1. **Mode A (quadrant I)**: electrical energy is transferred from $V_1$ side to $V_2$ side.
2. **Mode B (quadrant II)**: electrical energy is transferred from $V_2$ side to $V_1$ side.
3. **Mode C (quadrant III)**: electrical energy is transferred from $V_1$ side to $-V_2$ side.
4. **Mode D (quadrant IV)**: electrical energy is transferred from $-V_2$ side to $V_1$ side.

Each mode has two states: *on* and *off*. The switch/diode status of each state are shown in Table 5.3.

### 5.3.1 Mode A

Mode A is a ZVS buck converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.7. There are four time regions for the switch-off and -on period. The conduction duty cycle is $kT = (t_3 + t_4)$ when

![Equation Image]

<table>
<thead>
<tr>
<th>Mode</th>
<th>$f$(kHz)</th>
<th>$L_{m}$=$L_{r}$ ($\mu$H)</th>
<th>$C_r$ ($\mu$F)</th>
<th>$I_{i}$ (A)</th>
<th>$I_{o}$ (A)</th>
<th>$P_i$ (W)</th>
<th>$P_o$ (W)</th>
<th>$\eta$ (%)</th>
<th>PD(W/in$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>20.5</td>
<td>1</td>
<td>4</td>
<td>16.98</td>
<td>25</td>
<td>713</td>
<td>700</td>
<td>98.2</td>
<td>17.66</td>
</tr>
<tr>
<td>A</td>
<td>21</td>
<td>1</td>
<td>4</td>
<td>17.4</td>
<td>25</td>
<td>730.6</td>
<td>700</td>
<td>95.8</td>
<td>17.88</td>
</tr>
<tr>
<td>A</td>
<td>21.5</td>
<td>1</td>
<td>4</td>
<td>17.81</td>
<td>25</td>
<td>748</td>
<td>700</td>
<td>93.5</td>
<td>18.1</td>
</tr>
<tr>
<td>B</td>
<td>16.5</td>
<td>1</td>
<td>4</td>
<td>25</td>
<td>16.4</td>
<td>25</td>
<td>700</td>
<td>688.8</td>
<td>98.4</td>
</tr>
<tr>
<td>B</td>
<td>17</td>
<td>1</td>
<td>4</td>
<td>25</td>
<td>16.2</td>
<td>25</td>
<td>700</td>
<td>680.4</td>
<td>97.2</td>
</tr>
<tr>
<td>B</td>
<td>17.5</td>
<td>1</td>
<td>4</td>
<td>25</td>
<td>15.97</td>
<td>25</td>
<td>700</td>
<td>670.1</td>
<td>95.8</td>
</tr>
<tr>
<td>C</td>
<td>19</td>
<td>1</td>
<td>4</td>
<td>16.17</td>
<td>23.82</td>
<td>35</td>
<td>679.1</td>
<td>667</td>
<td>98.2</td>
</tr>
<tr>
<td>C</td>
<td>19.3</td>
<td>1</td>
<td>4</td>
<td>16.42</td>
<td>23.64</td>
<td>35</td>
<td>689.7</td>
<td>662</td>
<td>96</td>
</tr>
<tr>
<td>C</td>
<td>19.5</td>
<td>1</td>
<td>4</td>
<td>16.59</td>
<td>23.53</td>
<td>35</td>
<td>696.8</td>
<td>658.8</td>
<td>94.5</td>
</tr>
<tr>
<td>D</td>
<td>40</td>
<td>1</td>
<td>4</td>
<td>24.05</td>
<td>15.64</td>
<td>35</td>
<td>663.4</td>
<td>656.4</td>
<td>97.5</td>
</tr>
<tr>
<td>D</td>
<td>40.3</td>
<td>1</td>
<td>4</td>
<td>24.23</td>
<td>15.49</td>
<td>35</td>
<td>678.5</td>
<td>650.6</td>
<td>95.9</td>
</tr>
<tr>
<td>D</td>
<td>40.5</td>
<td>1</td>
<td>4</td>
<td>24.35</td>
<td>15.4</td>
<td>35</td>
<td>681.8</td>
<td>646.7</td>
<td>94.8</td>
</tr>
</tbody>
</table>
FIGURE 5.6
Four-quadrant DC/DC ZVS quasi-resonant Luo-converter.

TABLE 5.3
Switch Status

<table>
<thead>
<tr>
<th>Circuit / Switch or Diode</th>
<th>Mode A (Q-I)</th>
<th>Mode B (Q-II)</th>
<th>Mode C (Q-III)</th>
<th>Mode D (Q-IV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit</td>
<td>State-on</td>
<td>State-off</td>
<td>State-on</td>
<td>State-off</td>
</tr>
<tr>
<td>Circuit 1</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Circuit 2</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

Note: The blank status means off.
Multiple-Quadrant Soft-Switch Converters

The input current flows through the switch \( S_1 \) and the main inductor \( L \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_r - C_{r1} \).

The resonance frequency is

\[
\omega = \frac{1}{\sqrt{L_r C_{r1}}} \tag{5.60}
\]

and the normalized impedance is

\[
Z_1 = \frac{L_r}{\sqrt{C_{r1}}} \tag{5.61}
\]

The resonant voltage (AC component) is

\[
v_{c_1}(t) = Z_1 I_L \sin(\omega t + \alpha_c) \tag{5.62}
\]

Considering the DC component \( V_1 \), the peak voltage is

\[
v_{c1\text{-peak}} = V_1 + Z_1 I_L \tag{5.63}
\]
5.3.1.1 Interval \( t = 0 \) to \( t_1 \)
Switch \( S_1 \) turns off at \( t = 0 \), the capacitor voltage \( v_{C1} \) increases linearly with the slope \( I_1/C_{rl} \); this is the voltage linear rising interval. This voltage is smaller than the source voltage \( V_1 \). Therefore, no current flows through the diode \( D_2 \).

When \( t = t_1 \), it is equal to \( V_1 \). Therefore, the time is

\[
t_1 = \frac{V_1 C_{rl}}{I_1}
\]

(5.64)

and corresponding angular position is

\[
\alpha_1 = \sin^{-1}\left(\frac{V_1}{Z_1 I_1}\right)
\]

(5.65)

5.3.1.2 Interval \( t = t_1 \) to \( t_2 \)
In this period, since the voltage \( v_{C1} \) is higher than source voltage \( V_1 \), the current flows through the diode \( D_2 \). Circuit \( L_r - C_{rl} \) resonates; this is the resonance interval. The voltage waveform is a sinusoidal function. After its peak value \( v_{C1-peak} \), it descends down to zero \( (t = t_2) \). If the converter works in subresonance state, switch \( S_1 \) turns on at \( t = t_2 \). At this point we can see that the switch \( S_1 \) turns off and on at zero voltage condition. This period length is

\[
t_2 = \frac{1}{\omega_1} (\pi + \alpha_1)
\]

(5.66)

Simultaneously, the current \( i \) flows through the inductor \( L_r \), it is a sinusoidal function as well. When \( t = t_2 \), the corresponding value \( i_{r01} \) of the inductor current \( i \) is

\[
i_{r01} = -I_L \sin(\pi/2 + \alpha_1) = -I_L \cos \alpha_1
\]

(5.67)

5.3.1.3 Interval \( t = t_2 \) to \( t_3 \)
Since the diode \( D_1 \) does not allow the resonant voltage \( v_{C1} \) to become a negative value, then \( v_{C1} = 0 \). The free-wheeling diode \( D_2 \) conducts and the current \( i \) increases linearly with the slope \( V_1/I_r \); this is the linear recovering interval. Because load current \( I_1 \) is a constant current the current \( i \) increases linearly from \( i_{r01} \) to 0 at \( t = t_3 \), and \( i_{r01} = I_1 \) at \( t = t_3 \).

\[
t_3 = -\frac{i_{r01} L_r}{V_1}
\]

(5.68)

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5.3.1.4 Interval \( t = t_3 \) to \( t_4 \)

In this period the load current is supplied by the source. Diode \( D_2 \) is blocked until \( t = t_4 \); this is the normal on interval. The output current is equal to the main inductor current \( I_L \), so the average input current \( I_i \) is

\[
I_i = \frac{I_1 V_2}{V_1} = \frac{1}{T} \int_{t_3}^{t_4} i(t) dt = \frac{1}{T} \left( I_1 t_4 \right) = \frac{t_4}{T} I_1
\]

Therefore,

\[
t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1}
\]

We have the conduction duty

\[
k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4}
\]

The whole repeating period is

\[
T = t_1 + t_2 + t_3 + t_4
\]

and corresponding frequency is

\[
f = 1 / T
\]

5.3.2 Mode B

Mode B is a ZVS boost converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.8. There are four time regions for the switch-off and -on period. The conduction duty cycle is \( kT = (t_3 + t_4) \), but the output current only flows through the source \( V_1 \) in the period \( t_4 \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_r - C \).
The resonance frequency is

\[ \omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \]  

(5.75)

and the normalized impedance is

\[ Z_2 = \frac{L_r}{\sqrt{C_{r2}}} \]  

(5.76)

The resonant voltage (AC component) is

\[ v_{c2}(t) = Z_2 I_L \sin(\omega_2 t + \alpha_2) \]  

(5.77)

Considering the DC component \( V_1 \), the peak current is

\[ v_{c2\text{-peak}} = V_1 + Z_2 I_L \]  

(5.78)
5.3.2.1 Interval \( t = 0 \) to \( t_1 \)
Switch \( S_2 \) turns off at \( t = 0 \), the capacitor voltage \( v_{c2} \) increases linearly with the slope \( \frac{I_L}{C_{r2}} \). This voltage is equal to \( V_1 \) when \( t = t_1 \).

\[
t_1 = \frac{V_1 C_{r2}}{I_L}
\]

(5.79)

and corresponding angular position is

\[
\alpha_2 = \sin^{-1}\left(\frac{V_1}{Z_2 I_L}\right)
\]

(5.80)

5.3.2.2 Interval \( t = t_1 \) to \( t_2 \)
In this period the voltage \( v_{c2} \) is higher than the source voltage \( V_1 \). Circuit \( L_r C_{r2} \) resonates. The voltage waveform is a sinusoidal function. After its peak value, it descends down to 0 when \( t = t_2 \). If the converter works in subresonance state, switch \( S_2 \) turns on at \( t = t_2 \). Until this point we can see that the switch \( S_2 \) turns-off and -on at zero voltage condition. This period length is

\[
t_2 = \frac{1}{\omega_2} (\pi + \alpha_2)
\]

(5.81)

Simultaneously, the inductor current \( i_r \) flows through inductor \( L_r \), it is a sinusoidal function as well. When \( t = t_2 \), the corresponding value \( i_{r02} \) of the inductor current \( i_r \) is

\[
i_{r02} = I_L [1 + \sin(\pi / 2 + \alpha_2)] = I_L (1 + \cos \alpha_2)
\]

(5.82)

5.3.2.3 Interval \( t = t_2 \) to \( t_3 \)
Since the diode \( D_2 \) does not allow the resonant voltage to become a negative value, the voltage across the capacitor \( C_{r2} \) will be 0. The inductor current \( i_r \) decreases linearly with the slope \(-V_1/L_r\). Because load current \( I_L \) is a constant current, the current \( i_r \) decreases linearly from \( i_{r02} \) to \( I_L \) at \( t = t'_3 \), and \( i_r = 0 \) at \( t = t_3 \).

\[
t'_3 = \frac{(i_{r02} - I_L)L_r}{V_1}
\]

(5.83)

\[
t_3 = \frac{i_{r02} L_r}{V_1}
\]

(5.84)
5.3.2.4 Interval \( t = t_3 \) to \( t_4 \)

In this period the switch \( S_2 \) is on. Load current \( I_L \) does not flow through the source. Ignoring the power losses, and \( I_2 = I_L \) we have the output average current \( I_1 \):

\[
I_1 = \frac{I_1 V_2}{V_1} = \frac{1}{T} \int_{t_3}^{t_4} i_1 dt = \frac{1}{T} [I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L \tag{5.85}
\]

or

\[
\frac{V_2}{V_1} = \frac{1}{T} (t_2 + t_3) = \frac{t_2 + t_3}{t_1 + t_2 + t_3 + t_4} \tag{5.86}
\]

Therefore,

\[
t_4 = (\frac{V}{V_2} - 1)(t_2 + t_3) - t_1 \tag{5.87}
\]

We have the conduction duty

\[
k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \tag{5.88}
\]

The whole repeating period is

\[
T = t_1 + t_2 + t_3 + t_4 \tag{5.89}
\]

and corresponding frequency is

\[
f = 1 / T \tag{5.90}
\]

5.3.3 Mode C

Mode C is a ZVS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.9. There are four time regions for the switch-off and -on period. The conduction duty cycle is \( kT = (t_3 + t_4) \) when the input current \( I_i \) flows through the switch \( S_1 \) and the main inductor \( L \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_r - C_r \).
The resonance frequency is

\[ \omega_i = \frac{1}{\sqrt{L_r C_{rl}}} \]  \hspace{1cm} (5.91)

and the normalized impedance is

\[ Z_i = \frac{L_r}{\sqrt{C_{rl}}} \]  \hspace{1cm} (5.92)

The resonant voltage (AC component) is

\[ v_{c1}(t) = Z_i I_L \sin(\omega_i t + \alpha) \]  \hspace{1cm} (5.93)

Considering the DC component \( V_1 \), the peak voltage is

\[ v_{c1-peak} = V_1 + V_2 + Z_i I_L \]  \hspace{1cm} (5.94)
5.3.3.1 Interval \( t = 0 \) to \( t_1 \)
Switch \( S_1 \) turns off at \( t = 0 \), the capacitor voltage \( v_{C1} \) increases linearly with the slope \( I_L/C_{r1} \). This voltage \( v_{C1} \) is smaller than \((V_1 + V_2)\). Therefore, no current flows through the diode \( D_2 \). When \( t = t_1 \), it is equal to \((V_1 + V_2)\). Therefore,

\[
t_1 = \frac{(V_1 + V_2)C_{r1}}{I_L} \tag{5.95}
\]

and corresponding angular position is

\[
\alpha_1 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_{r1}I_L}\right) \tag{5.96}
\]

5.3.3.2 Interval \( t = t_1 \) to \( t_2 \)
In this period, since the voltage \( v_{C1} \) is higher than source voltage \( V_1 \), the current flows through the diode \( D_2 \). Circuit \( L_r - C_{r1} \) resonates. The voltage waveform is a sinusoidal function. After its peak value \( v_{C1,\text{peak}} \), it descends down to zero \((t = t_2)\). If the converter works in subresonance state, switch \( S_1 \) turns on at \( t = t_2 \). This period length is

\[
t_2 = \frac{1}{\omega_1} (\pi + \alpha_1) \tag{5.97}
\]

Simultaneously, the current \( i_r \) flows through the inductor \( L_r \), it is a sinusoidal function as well. When \( t = t_2 \), the corresponding value \( i_{rO1} \) of the inductor current \( i_r \) is

\[
i_{rO1} = -I_L \sin(\pi/2 + \alpha_1) = -I_L \cos \alpha_1 \tag{5.98}
\]

5.3.3.3 Interval \( t = t_2 \) to \( t_3 \)
Since the diode \( D_1 \) does not allow the resonant voltage \( v_{C1} \) to become a negative value, then \( v_{C1} = 0 \). The free-wheeling diode \( D_2 \) conducts and the current \( i \) increases linearly with the slope \((V_1 + V_2)/L_r\). Because load current \( I_L \) is a constant current the current \( i \) increases linearly from \( i_{rO1} \) to 0 at \( t = t_3 \) and \( i_{rO1} = I_L \) at \( t = t_3 \).

\[
t_3' = \frac{i_{rO1}L_r}{V_1 + V_2} \tag{5.99}
\]

and

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5.3.3.4 **Interval** \( t = t_3 \) to \( t_4 \)

In this period the load current is supplied by the source. Diode \( D_2 \) is blocked until \( t = t_4 \). The output current is equal to the main inductor current \( I_L \), so the average input current \( I_1 \) is

\[
I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T} \int_{t_3}^{t_4} i_i dt = \frac{1}{T} (I_L t_4) = \frac{t_4}{T} I_L
\]

and

\[
I_2 = \frac{1}{T} \int_{t_3}^{t_5} (I_L - i_i) dt = \frac{t_5 + t_3}{T} I_L
\]

Therefore,

\[
t_4 = \frac{V_2(t_2 + t_3)}{V_1}
\]

We have the conduction duty

\[
k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4}
\]

The whole repeating period is

\[
T = t_1 + t_2 + t_3 + t_4
\]

and corresponding frequency is

\[
f = 1 / T
\]

5.3.4 **Mode D**

Mode D is a cross ZVS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in Figure 5.10. There are four time regions
for the switch-off and -on period. The conduction duty cycle is \( kT = (t_3 + t_4) \), but the output current only flows through the source \( V_1 \) in the period \( t_4 \). The whole period is \( T = (t_1 + t_2 + t_3 + t_4) \). The resonance circuit is \( L_r-C_{r2} \).

The resonance frequency is

\[
\omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \quad (5.107)
\]

and the normalized impedance is

\[
Z_2 = \frac{L_r}{\sqrt{C_{r2}}} \quad (5.108)
\]

The resonant voltage (AC component) is

\[
v_{c2}(t) = Z_2 I_L \sin(\omega_2 t + \alpha_2) \quad (5.109)
\]

Considering the DC component \( V_1 \), the peak current is
5.3.4.1 Interval $t = 0$ to $t_1$

Switch $S_2$ turns off at $t = 0$, the capacitor voltage $v_{c_2}$ increases linearly with the slope $I_1/C_{r_2}$. It is equal to $(V_1 + V_2)$ when $t = t_1$.

$$t_1 = \frac{(V_1 + V_2)C_{r_2}}{I_1} \tag{5.111}$$

and corresponding angular position is

$$\alpha_2 = \sin^{-1}(\frac{V_1 + V_2}{Z_2I_1}) \tag{5.112}$$

5.3.4.2 Interval $t = t_1$ to $t_2$

In this period the voltage $v_{c_2}$ is higher than the sum-voltage $(V_1 + V_2)$. Circuit $L_r - C_{r_2}$ resonates. The voltage waveform is a sinusoidal function. After its peak value, it descends down to 0 when $t = t_2$. If the converter works in subresonance state, switch $S_2$ turns on at $t = t_2$. This period length is

$$t_2 = \frac{1}{\omega_2} (\pi + \alpha_2) \tag{5.113}$$

Simultaneously, the inductor current $i_r$ flows through inductor $L_r$, it is a sinusoidal function as well. When $t = t_2$, the corresponding value $i_{rO2}$ of the inductor current $i_r$ is

$$i_{rO2} = I_1[1 + \sin(\pi/2 + \alpha_2)] = I_1(1 + \cos \alpha_2) \tag{5.114}$$

5.3.4.3 Interval $t = t_2$ to $t_3$

Since the diode $D_2$ does not allow the resonant voltage to become a negative value, the voltage across the capacitor $C_{r_2}$ will be 0. The inductor current $i_r$ decreases linearly with the slope $-(V_1 + V_2)/L_r$. Because the main inductor current $I_1$ is a constant current, the current $i_r$ decreases linearly from $i_{rO2}$ to $I_1$ at $t = t_2$ and $i_r = 0$ at $t = t_3$.

$$t_3' = \frac{(I_{rO2} - I_1)L_r}{V_1 + V_2} \tag{5.115}$$
\[
t_3 = \frac{i_{o2}L_2}{V_1 + V_2}
\]

(5.116)

### 5.3.4.4 Interval \( t = t_3 \) to \( t_4 \)

In this period since the switch \( S_2 \) is on, the main inductor current \( I_L \) does not flow through the source. Ignoring the power losses, we have the output average current \( I_1 \):

\[
I_1 = \frac{1}{T} \int_{t_3}^{t_4} i_L dt = \frac{1}{T} [I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L
\]

(5.117)

and

\[
I_2 = \frac{1}{T} \int_{t_3}^{t_4} i_L dt = \frac{1}{T} (I_L t_4) = \frac{t_4}{T} I_L
\]

(5.118)

Therefore,

\[
t_4 = \frac{V_1}{V_2} (t_2 + t_3)
\]

(5.119)

We have the conduction duty

\[
k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4}
\]

(5.120)

The whole repeating period is

\[
T = t_1 + t_2 + t_3 + t_4
\]

(5.121)

and corresponding frequency is

\[
f = 1 / T
\]

(5.122)
### 5.3.5 Experimental Results

A testing rig with a battery of ±28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are: $V_1 = 42$ V and $V_2 = ±28$ V, $L = 30$ μH, $L_r = 4$ μH, $C_{r1} = C_{r2} = 1$ μF; the volume is 40 in³. The experimental results are shown in Table 5.4. The average power transfer efficiency is higher than 96%, and total average PD is 17.6 W/in³. This figure is much higher than that of the classical converters whose PD is usually less than 5 W/in³. Since the switch frequency is low ($f < 56$ kHz) and this converter works at the mono-resonance frequency, the components of the high-order harmonics are small. Applying FFT analysis, the THD is very small, so that the EMI is weak, and the EMS and EMC are reasonable.

### 5.4 Multiple-Quadrant Zero-Transition DC/DC Luo-Converters

Zero-transition (ZT) technique significantly reduces the power losses across the switches during switch-on and -off. Unfortunately, the literature discusses the converters only working at single quadrant operation. The four-quadrant ZT DC/DC Luo-converters perform soft switch four-quadrant operation without significant voltage and current stresses. They effectively reduce the power losses and greatly increase the power transfer efficiency. These converters are shown in Figure 5.11a and b. Circuit 1 implements the operation in quadrants I and II, circuit 2 implements the operation in quadrants III and IV. Circuit 1 and circuit 2 can be converted each other via an auxiliary switch. Each circuit consists of one main inductor $L$ and two main

<table>
<thead>
<tr>
<th>Mode</th>
<th>$f$(kHz)</th>
<th>$L_r$(μH)</th>
<th>$C_{r1} = C_{r2}$(μF)</th>
<th>$I_{r1}$(A)</th>
<th>$I_{r2}$(A)</th>
<th>$P_r$(W)</th>
<th>$P_o$(W)</th>
<th>$\eta$(%)</th>
<th>PD(W/in³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>23</td>
<td>4</td>
<td>1</td>
<td>17.16</td>
<td>25</td>
<td>720.8</td>
<td>700</td>
<td>97.1</td>
<td>17.76</td>
</tr>
<tr>
<td>A</td>
<td>23.5</td>
<td>4</td>
<td>1</td>
<td>16.99</td>
<td>25</td>
<td>713.7</td>
<td>700</td>
<td>98.1</td>
<td>17.67</td>
</tr>
<tr>
<td>A</td>
<td>24</td>
<td>4</td>
<td>1</td>
<td>16.82</td>
<td>25</td>
<td>706.6</td>
<td>700</td>
<td>99</td>
<td>17.58</td>
</tr>
<tr>
<td>B</td>
<td>54</td>
<td>4</td>
<td>1</td>
<td>25</td>
<td>16.13</td>
<td>25</td>
<td>700</td>
<td>677.6</td>
<td>96.8</td>
</tr>
<tr>
<td>B</td>
<td>54.5</td>
<td>4</td>
<td>1</td>
<td>25</td>
<td>16.28</td>
<td>25</td>
<td>700</td>
<td>683.8</td>
<td>97.7</td>
</tr>
<tr>
<td>B</td>
<td>55</td>
<td>4</td>
<td>1</td>
<td>25</td>
<td>16.43</td>
<td>25</td>
<td>700</td>
<td>690.1</td>
<td>98.6</td>
</tr>
<tr>
<td>C</td>
<td>44</td>
<td>4</td>
<td>1</td>
<td>17.64</td>
<td>24.27</td>
<td>45</td>
<td>740.9</td>
<td>679.6</td>
<td>91.7</td>
</tr>
<tr>
<td>C</td>
<td>44.5</td>
<td>4</td>
<td>1</td>
<td>17.32</td>
<td>24.55</td>
<td>45</td>
<td>727.6</td>
<td>687.5</td>
<td>94.5</td>
</tr>
<tr>
<td>C</td>
<td>45</td>
<td>4</td>
<td>1</td>
<td>17.01</td>
<td>24.83</td>
<td>45</td>
<td>714.5</td>
<td>695.2</td>
<td>97.3</td>
</tr>
<tr>
<td>D</td>
<td>29.5</td>
<td>4</td>
<td>1</td>
<td>26.65</td>
<td>16.27</td>
<td>45</td>
<td>746.3</td>
<td>683.5</td>
<td>91.6</td>
</tr>
<tr>
<td>D</td>
<td>30</td>
<td>4</td>
<td>1</td>
<td>26.34</td>
<td>16.55</td>
<td>45</td>
<td>737.6</td>
<td>695.1</td>
<td>94.2</td>
</tr>
<tr>
<td>D</td>
<td>30.5</td>
<td>4</td>
<td>1</td>
<td>26.28</td>
<td>16.83</td>
<td>45</td>
<td>735.9</td>
<td>706.7</td>
<td>96</td>
</tr>
</tbody>
</table>
Advanced Multi-Quadrant Operation DC/DC Converters

switches. The source and load voltages are usually constant, e.g., \( V_1 = 42 \text{ V} \) and \( V_2 = \pm 28 \text{ V} \). There are four modes of operation:

1. Mode A (quadrant I): electrical energy is transferred from \( V_1 \) side to \( V_2 \) side.
2. Mode B (quadrant II): electrical energy is transferred from \( V_2 \) side to \( V_1 \) side.
3. Mode C (quadrant III): electrical energy is transferred from \( V_1 \) side to \( -V_2 \) side.
4. Mode D (quadrant IV): electrical energy is transferred from \( -V_2 \) side to \( V_1 \) side.

Each mode has two states: on and off. The switch and diode status of each state for modes A and B are shown in Table 5.5; the status of each state for modes C and D are shown in Table 5.6. The equivalent circuits for modes A, B, C, and D are shown in Figures 5.12, 5.14, 5.16, and 5.18. The corresponding waveforms for each mode are shown in Figures 5.13, 5.15, 5.17, and 5.19 respectively.
### TABLE 5.5
Switch/Diode Status

<table>
<thead>
<tr>
<th>S &amp; D</th>
<th>Mode A (Q₁)</th>
<th>Mode B (Q₂)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Δt₁</td>
<td>Δt₂</td>
</tr>
<tr>
<td>S₁</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>D₁</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S₃</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D₃</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: The blank status means off referring to circuit 1 of Figure 5.11a.

### TABLE 5.6
Switch/Diode Status

<table>
<thead>
<tr>
<th>S &amp; D</th>
<th>Mode C (Q₃)</th>
<th>Mode D (Q₄)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Δt₁</td>
<td>Δt₂</td>
</tr>
<tr>
<td>S₁</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>D₁</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S₃</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D₃</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: The blank status means off referring to circuit 2 of Figure 5.11b.

![FIGURE 5.12](https://www.IranSwitching.ir)

Mode A (Q₁) operation.
5.4.1 Mode A (Quadrant I Operation)

Mode A performs quadrant I operation. The equivalent circuit for Mode A, is shown in Figure 5.12. The corresponding waveforms are shown in Figure 5.13.

Stage 1 \((t_0 - t_1)\): prior to \(t_0\), \(S_1\) and \(S_a\) are all off. The circuit current is freewheeling through the antiparallel diode \(D_b\) and \(D_2\). \(C_r\) voltage is zero, \(I_L = I_{Lr} + I_{D2}\). At \(t_0\), the auxiliary switch \(S_a\) is turned on with zero current. Capacitor \(C_r\) is charged in reverse, so that diode \(D_b\) is reverse-biased in soft commutation. The current of \(L_r\) decreases linearly while the current of \(S_a\) increases gradually. At \(t = t_1\), the current of \(L_r\) falls to zero; \(D_2\) is turned off with soft commutation. Meanwhile, current of \(S_a\) reaches to \(I_L\). The current of resonant inductor \(L_r\) is

\[
i_{Lr} = \frac{V_r}{L_r} t
\]

The time interval of the first stage \(\Delta t_1\) is given by equation

\[
\Delta t_1 = \frac{I_1 L_r}{V_r}
\]  

(5.123)

Stage 2 \((t_1 - t_3)\): the main switch \(S_1\) junction capacitor \(C_j\) (not shown in Figure 5.12) discharges through \(L_r\), \(S_a\). Capacitor \(C_r\) also discharges through \(L_r\). \(V_{cr}\) and \(V_{ds}\) fall to zero rapidly at \(t_2\). Thereafter, the antiparallel diode of \(S_1\) starts to conduct and a small reverse current flows through \(L_r\). The resonant time interval of stage 2, \(\Delta t_2\), is given by

\[
www.IranSwitching.ir
Stage 3 \((t_3 - t_4)\): at \(t_3\), \(S_1\) is turned on with zero current and zero voltage. At the same moment, turn off \(S_a\). It should be noted that the turn on/off point is not critical. \(S_1\) and \(S_a\) could be turn on and off prior to \(t_2\). If so, \(t_2\) does not exist in the stage. Therefore,

\[
\Delta t_3 = t_{S_a\text{-on}} - \Delta t_1 - \Delta t_2
\]  

Stage 4 \((t_3 - t_4)\): when \(S_a\) is turned off, \(i_L\) charges \(C_r\) and \(L_r\) through the conducted \(S_1\). The voltage of \(C_r\) increases gradually, enabling \(S_a\) to be turned off with zero voltage. After \(i_{Lr}\) reaches \(i_{Lr}\), capacitor \(C_r\) starts to discharge through \(L_r\). At \(t = t_{Lr}\), \(V_{Lr}\) reaches zero again.

\[
\Delta t_4 = \frac{V_{C_r}}{I_{Lr}}
\]  

Stage 5 \((t_4 - t_5)\): During this period, the circuit current flows through main switch \(S_1\), and inductor \(L_r, L\), like the conventional PWM converter. The length is determined by the control of the PWM signal.

\[
\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r}
\]  

Stage 6 \((t_5 - t_6)\): at \(t_5\), main switch \(S_1\) is turned off. Inductor and capacitor \(C_r\) are in resonance. The voltage of \(C_r\) increases gradually at first, so that the voltage across the main switch \(S_1\) rises gradually. \(S_1\) is therefore turned off with zero voltage. At \(t_{Lr}\), the voltage of \(C_r\) becomes zero; \(D_2\) and \(D_b\) start to conduct. The time interval is given by

\[
\Delta t_6 = kT - \Delta t_4 - \Delta t_5
\]  

Stage 7 \((t_6 - t_7)\): During this period, the circuit current is freewheeling through \(D_2\) and \(D_{Lr}\) like the conventional PWM converter.

\[
\Delta t_7 = \frac{\pi}{2} \sqrt{L_r C_r}
\]  

Stage 8 \((t_7 - t_8)\): at \(t_{Lr}\), \(S_a\) is turned on once more, to start the next switch cycle. The length of this period is determined by the control of the PWM.

\[
\Delta t_8 = (1 - k)T - t_{S_a\text{-on}} - \Delta t_7
\]
5.4.2 Mode B (Quadrant II Operation)

Mode B performs quadrant II operations. The equivalent circuit for mode B, is shown in Figure 5.14. The operational process is analogous to mode A operation. The corresponding waveforms are shown in Figure 5.15. The calculation formulae for mode B are listed below:

\[
\Delta t_1 = \frac{I \cdot L_r}{V_1}, \quad \Delta t_2 = \frac{\pi}{2} \sqrt{\frac{L_r C_j}{I_L}}, \\
\Delta t_3 = t_{5b-on} - \Delta t_1 - \Delta t_2, \quad \Delta t_4 = \frac{V_1 C_j}{I_L}
\]
5.4.3 Mode C (Quadrant III Operation)

Mode C performs quadrant III operation. The equivalent circuit for mode C, is shown in Figure 5.16. The operational process is analogous to mode A operation. The corresponding waveforms are shown in Figure 5.17. The calculation formulae of mode C are listed below:

\[
\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r} \quad \Delta t_6 = kT - \Delta t_4 - \Delta t_5
\]

\[
\Delta t_7 = \pi \sqrt{L_r C_r} \quad \Delta t_8 = (1 - k)T - t_{Sb-on} - \Delta t_7
\]

FIGURE 5.16
Mode C (Q_III) operation.

FIGURE 5.17
Waveforms of mode C (Q_III).
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5.4.4 Mode D (Quadrant IV Operation)

Mode D performs in quadrant IV operation. The equivalent circuit for mode D, is shown in Figure 5.18. The operational process is analogous to mode B operation. The corresponding waveforms are shown in Figure 5.19. The calculation formulae of mode D are listed below:

\[
\Delta t_1 = \frac{I_L L_r}{V_1 + V_2} \quad \Delta t_2 = \frac{\pi}{2} \sqrt{L_r C_r} \\
\Delta t_3 = t_{Sa-on} - \Delta t_1 - \Delta t_2 \quad \Delta t_4 = \frac{V_1 + V_2}{I_L} C_r \\
\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r} \quad \Delta t_6 = kT - \Delta t_4 - \Delta t_5 \\
\Delta t_7 = \pi \sqrt{L_r C_r} \quad \Delta t_8 = (1 - k)T - t_{Sa-on} - \Delta t_7
\]
5.4.5 Simulation Results

PSpice is a popular simulation method to test and verify electronic circuit design. In order to implement this ZV-ZCS two-quadrant DC/DC converter with 3 kW delivery, the rig of a modern car battery ±28 VDC as a load and a 42 VDC as a source power supply was tested. The testing conditions are:

\[ V_1 = 42 \text{ V} \quad \text{and} \quad V_2 = 28 \text{ V}, \quad L_r = 2 \mu\text{H}, \quad C_r = 0.8 \text{ nF}, \quad \text{and} \quad L = 550 \mu\text{H}, \quad f = 100 \text{ kHz}. \]

The simulation result for Q_I is shown in Figure 5.20, the simulation result for Q_II is shown in Figure 5.21. From these waveform and data, we can see that the main switches in the converter are switched on at ZC and ZVS condition; switched off at ZVS condition. Moreover, all the auxiliary switches and diode are operated under soft commutation. The testing conditions are:

\[ V_1 = 42 \text{ V} \quad \text{and} \quad V_2 = -28 \text{ V}, \quad L_r = 2 \mu\text{H}, \quad C_r = 0.8 \text{ nF}, \quad \text{and} \quad L = 550 \mu\text{H}, \quad f = 100 \text{ kHz}. \]

The simulation results for Q_III are shown in Figure 5.22, the simulation results for Q_IV are shown in Figure 5.23. From these waveforms we can see that the main switches in the converter are switched on at ZC and ZVS condition; switched off at ZVS condition. Moreover, all the auxiliary switches and diodes are operated under soft commutation.

5.4.6 Experimental Results

A testing rig battery of ±28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are:

\[ V_1 = 42 \text{ V} \quad \text{and} \quad V_2 = \pm 28 \text{ V}, \quad L = 30 \mu\text{H}, \quad L_1 = L_2 = 1 \mu\text{H}, \quad C = 4 \mu\text{F}, \quad I_L = 25 \text{ A} \] (for Q_I and Q_II), \(35 \text{ A} \) (for Q_III and Q_IV) and the volume is 40 in³. The experimental results are shown in Table 5.7. The average power transfer efficiency is higher than 89.7% and the total average PD is 17.5 W/in³. This figure is much higher than the classical converters whose PD is usually less than 5 W/in³. Since the switch
FIGURE 5.20
Simulation result for ZV-ZCS mode A operation ($f = 100$ kHz; $k = 30\%$).

FIGURE 5.21
Simulation result for ZV-ZCS mode B operation ($f = 100$ kHz; $k = 60\%$).
FIGURE 5.22
Simulation result for ZV-ZCS mode C operation ($f = 100$ kHz; $k = 30\%$).

FIGURE 5.23
Simulation result for ZV-ZCS mode D operation ($f = 100$ kHz; $k = 70\%$).
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The frequency and conduction duty $k$ can be adjusted individually, we chose $f = 100$ kHz and a suitable conduction duty cycle $k$ to obtain the proper operation state.

5.4.7 Design Considerations

In a practical design, for ease of implementation, the control of the two switches can adopt the constant time-delay method:

1. Turn-on of the main switch should delay turn-on of the auxiliary switch at least by $T_{ON_{min}}$. The auxiliary switch could be turned off simultaneously with the turn-on of the main switch. But it is better to turn off $S_a$ shortly after turn-on of the main switch to secure soft turnoff of the auxiliary switch.

2. For prompt soft turn-off of main switch ($S_1$ or $S_2$) and energy recovery, turn-off of the auxiliary switch should precede turn-off of the main switch by a minimum time of $T_{OFF_{min}}$. This means that for prompt soft switch, the above constraint should be met under the minimum duty cycle $k_{min}$. The simple timing constraints are calculated as follows:

$$T_D \geq T_{ON_{min}} = \Delta t_1 + \Delta t_2 = \frac{I_1 L_2}{V_1} + \frac{\pi}{2} \sqrt{L_j C_j}$$  \hspace{1cm} (5.131)

$$T_P \geq T_{OFF_{min}} = \frac{C_j V_1}{I_p} + \frac{L_j}{V_1} I_p$$  \hspace{1cm} (5.132)

$$i_p = \sqrt{I_L^2 + \frac{V_1^2}{\rho}} \quad \rho = \sqrt{\frac{L_j}{C_j}}$$  \hspace{1cm} (5.133)

<table>
<thead>
<tr>
<th>Mode</th>
<th>$f$ (kHz)</th>
<th>$L_{r1}$ ($\mu$H)</th>
<th>$C_r$ ($\mu$F)</th>
<th>$I_r$ (A)</th>
<th>$I_p$ (A)</th>
<th>$P_r$ (W)</th>
<th>$P_o$ (W)</th>
<th>$\eta$ (%)</th>
<th>PD (W/in$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>20.5</td>
<td>1</td>
<td>4</td>
<td>16.98</td>
<td>25</td>
<td>713</td>
<td>700</td>
<td>98.2</td>
<td>17.66</td>
</tr>
<tr>
<td>A</td>
<td>21</td>
<td>1</td>
<td>4</td>
<td>17.4</td>
<td>25</td>
<td>730.6</td>
<td>700</td>
<td>95.8</td>
<td>17.88</td>
</tr>
<tr>
<td>A</td>
<td>21.5</td>
<td>1</td>
<td>4</td>
<td>17.81</td>
<td>25</td>
<td>748</td>
<td>700</td>
<td>93.5</td>
<td>18.1</td>
</tr>
<tr>
<td>B</td>
<td>16.5</td>
<td>1</td>
<td>4</td>
<td>25</td>
<td>16.4</td>
<td>700</td>
<td>688.8</td>
<td>98.4</td>
<td>17.36</td>
</tr>
<tr>
<td>B</td>
<td>17</td>
<td>1</td>
<td>4</td>
<td>25</td>
<td>16.2</td>
<td>700</td>
<td>680.4</td>
<td>97.2</td>
<td>17.25</td>
</tr>
<tr>
<td>B</td>
<td>17.5</td>
<td>1</td>
<td>4</td>
<td>25</td>
<td>15.97</td>
<td>700</td>
<td>670.1</td>
<td>95.8</td>
<td>17.13</td>
</tr>
<tr>
<td>C</td>
<td>18.3</td>
<td>1</td>
<td>4</td>
<td>16.24</td>
<td>24.03</td>
<td>35</td>
<td>682.1</td>
<td>672.8</td>
<td>98.6</td>
</tr>
<tr>
<td>C</td>
<td>18.5</td>
<td>1</td>
<td>4</td>
<td>16.42</td>
<td>23.91</td>
<td>35</td>
<td>689.6</td>
<td>669.4</td>
<td>97.1</td>
</tr>
<tr>
<td>C</td>
<td>18.7</td>
<td>1</td>
<td>4</td>
<td>16.59</td>
<td>23.79</td>
<td>35</td>
<td>696.8</td>
<td>666.1</td>
<td>95.6</td>
</tr>
<tr>
<td>D</td>
<td>37.2</td>
<td>1</td>
<td>4</td>
<td>24.42</td>
<td>16.02</td>
<td>35</td>
<td>683.8</td>
<td>672.7</td>
<td>98.4</td>
</tr>
<tr>
<td>D</td>
<td>37.5</td>
<td>1</td>
<td>4</td>
<td>24.62</td>
<td>15.87</td>
<td>35</td>
<td>689.4</td>
<td>666.4</td>
<td>96.7</td>
</tr>
<tr>
<td>D</td>
<td>37.8</td>
<td>1</td>
<td>4</td>
<td>24.81</td>
<td>15.71</td>
<td>35</td>
<td>694.7</td>
<td>660</td>
<td>95</td>
</tr>
</tbody>
</table>
Where $C_j$ is the junction capacitor across the main switch’s drain and source, $T_D$ is the time that turn-on of main switch delays turn-on of auxiliary switch. $T_P$ is the time that turn-off of auxiliary switch precedes turn-off of main switch. $i_p$ is $L_r$ peak current.

For engineering implementation, as no capacitor is directly paralleled with the main switch, the time interval $\Delta t$ is very small; moreover, the turn-on loss caused by the junction capacitor is minimum if the main switch is turned-on before $V_{ds}$ falls to zero. So, $\Delta t$ in Equation (5.131) can be ignored for simple design:

\[
T_D \geq T_{ON_{min}} = \Delta t_1 = \frac{I_p L_r}{V_1}
\]  

(5.134)

To secure the soft switch under minimum duty cycle $k_{min}$, Equation (5.132) can be expressed as:

\[
k_{min} T_s \geq \Delta T_{OFF_{min}} = \frac{C V_1}{i_p} + \frac{L_r}{V_1} i_p
\]  

(5.135)

To achieve the similar conversion ratios of its hard switch PWM counterpart, the commutation transition i.e., $\Delta T_{ON_{min}}$ is normally set as 10 to 15% cycle in practical design:

\[
T_{ON_{min}} = \frac{I_{L_{\text{max}}} L_r}{V_1} \leq (10\% - 15\%) T_s
\]  

(5.136)

From Equation (5.136) $L_r$ can be obtained, for practical implementation, turn-on of the main switch delays turn-on of the auxiliary switch a constant time $T_D$:

\[
T_D = \frac{I_{L_{\text{max}}} V_1}{V_1}
\]  

(5.137)

To reduce the auxiliary switch’s conduction loss, the auxiliary switch is turned off right after turn-on of the main switch. From Equation (5.133), it is obvious that the peak current of $L_r$ does not relate to $C_r$. So, $C_r$ can be set large enough to reduce the turn-off loss of the main switch most effectively. But $C_r$ should meet the constraint of Equation (5.135) as well.

Compared with other soft-switch circuits, besides the soft switch of the auxiliary switch, the proposed circuit possesses the simplicity in topology. Another merit is that $C_r$ is not directly paralleled with the main switch. It not only provides soft turn-off for all the switches, but also does not discharge to $L_r$. A lower peak current in the auxiliary switch could, therefore,
be expected, particularly in cases where a small snubber inductor is used in high-frequency operation. Moreover, as the charge of $C$, does not increase $L_r$ current, the design trade-off between $C$, and current stress on the auxiliary switch does not exist, and the design of $L_r$ and $C$, become easy, as the above design analysis indicates. Also, with the help of inductor $L_r$, the reverse-recovery current of the main diode is effectively minimized.

It should be also noted here that the turn-on point of the main switch is not critical. The main switch could be turned on prior to $t_2$, because the turn-on loss caused by the junction capacitor is very small.

The control principle adopted here is simple, as it does not need the cross-zero voltage detection of the main switch. So it is easy to implement, but it has its limitations in light-load or no-load operation. Since the duty cycle of the main switch may be smaller than the duty cycle of the auxiliary switch at no load or light load, the constant duty cycle of the auxiliary switch will charge up the output capacitor without control. In such a case, certain current or voltage cross-zero detection is required to adjust the duty cycle of the auxiliary switch. On the other hand, the conduction loss is increased, as the auxiliary switch is not optimized with the minimum conduction at light load by using this control method.

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ZVS. See Zero-voltage switch

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