Analysis and Design of a Push–Pull Quasi-Resonant Boost Power Factor Corrector

Yu-Kang Lo, Member, IEEE, Chung-Yi Lin, Huang-Jen Chiu, Senior Member, IEEE, Shih-Jen Cheng, and Jing-Yuan Lin

Abstract—This paper proposes a novel power-factor corrector (PFC), which is mainly composed of two-phase transition-mode (TM) boost-type power-factor correctors (PFCs) and a coupled inductor. By integrating two boost inductors into one magnetic core, not only the circuit volume is reduced, but also the operating frequency of the core is double of the switching frequency. Comparing with single-phase TM boost PFC, both the input and output current ripples of the proposed PFC can be reduced if the equivalent inductance of the coupled inductor equals the inductance of single-phase TM boost PFC. Therefore, both the power-factor value and the power density are increased. The proposed topology is capable of sharing the input current and output current equally. A cut-in-half duty cycle can reduce the conduction losses of the switches and both the turns and diameters of the inductor windings. The advantages of a TM boost PFC, such as quasi-resonant (QR) valley switching on the switch and zero-current switching (ZCS) of the output diode, are maintained to improve the overall conversion efficiency. Detailed analysis and design procedures of the proposed topology are given. Simulations and experiments are conducted on a prototype with a universal line voltage, a 380-V output dc voltage and a 200-W output power to verify its feasibility.

Index Terms—Coupled inductor, power factor corrector, push–pull topology, quasi-resonant (QR) converter.

I. INTRODUCTION

T
HE boost converter is probably the most popular topology adopted for a power factor corrector (PFC). A boost PFC converts the universal ac input voltage into a regulated dc output voltage, which supplies to the poststage power converter. It also improves the power factor (PF) and the input current harmonics. There are three operating modes of a boost PFC, namely, continuous conduction mode (CCM), discontinuous conduction mode (DCM), and transition mode (TM) [1]–[5]. CCM is suitable for high-power applications with significant input current level, especially at the low line input voltage. In addition to its advantages of reducing the current stresses of the semiconductor devices and the low current ripple, CCM also features the best PF correction performance among these operating modes. However, for the low power applications, the bulky inductor deteriorates the power density. Moreover, the hard switching of the switch and the reverse recovery problem of the output diode increases the switching losses. On the other hand, DCM has low input inductance and the output diode is turned OFF naturally with zero current, which is more appropriate for low power circuits. However, the harmonic contents of the input current are higher with DCM control. TM, with a moderate inductance and PF value, is a compromise between CCM and DCM. TM has one more advantage of quasi-resonant (QR) valley switching of the switch, which can decrease the turn-on losses.

To increase the power rating of a TM boost PFC to the medium level without raising the EMI issue and increasing the current stresses of the circuit elements, an interleaved TM boost PFC [6]–[14] is recently proposed. Derived from two TM boost converters with the interleaved operations, the power rating is increased and the input current and output current are shared equally with lower current ripples. Therefore, the total harmonic distortion (THD) of input current and the output capacitance can be reduced. However, the need of two inductors with two independent cores increases the circuit volume. In this paper, a push–pull boost PFC composed of two interleaved TM boost PFCs and a coupled inductor [15]–[19] is proposed. A single magnetic core is used. The two identical modules can share the output power and promote the power capability up to the medium-power-level applications. In addition, coupling the two distributed boost inductors into a single magnetic core substantially reduces the circuit volume and the cost, which are the important targets of the development of switching power supply today. The interleaved operations of the switches act like a push–pull converter [20], [21]. The difference is that the operating frequency of the core is double of the switching frequency, which means that not only the circuit volume is reduced, but also the operating frequency of the core is double of the switching frequency. Comparing with single-phase TM boost PFC, both the input and output current ripple of the proposed PFC can be reduced if the equivalent inductance of the coupled inductor equals the inductance of single-phase TM boost PFC. Therefore, both the PF value and the power density are increased. In addition to the equal distributions of the input current and output current, the proposed topology with a cut-in-half duty cycle can reduce the conduction losses of the switches and both the turns and diameters of the inductor windings. It also maintains the advantages of a TM boost PFC, such as QR valley switching on the switch [22]–[24] and zero-current switching (ZCS) of the output diode, to reduce the switching losses and improve the
conversion efficiency. In the following sections, the operating principles and the design procedures are described. Simulations are carried out and experimental results are measured for a 200-W prototype circuit. Finally, the comparisons between a TM boost PFC, an interleaved TM boost PFC, and the proposed topology are made to evaluate the pros and cons.

II. OPERATING PRINCIPLES

Fig. 1 shows the schematics of the proposed topology. Module A consists of the switch $S_a$, the winding $N_{Pa}$, the inductor $L_a$, and the output diode $D_a$. Module B consists of the switch $S_b$, the winding $N_{Pb}$, the inductor $L_b$, and the output diode $D_b$. These two modules have a common output capacitor $C_o$. $L_a$ and $L_b$ are two coupled windings wound on the same magnetic core. Theoretically, the same turns of these two windings will lead to the same inductances.

The proposed PFC is operated by the TM control with a constant on-time and variable switching frequencies. The key waveforms are drawn as in Fig. 2. To analyze the operating principles, there are some assumptions listed as follows.

1) The conducting resistances of $S_a$ and $S_b$ are ideally zero.

The conduction time interval is $DT_s$, where $D$ is the duty cycle and $T_s$ is the switching period.

2) The forward voltages of $D_a$ and $D_b$ are ideally zero.

3) The magnetic core for manufacturing $L_a$ and $L_b$ is perfectly coupled without leakage inductance. In addition, the turns of the windings $N_{Pa}$ and $N_{Pb}$ are the same. Therefore, $L_a$ and $L_b$ are also matched.

The operating states of the proposed topology are analyzed as follows.

State 1: $t_0 < t < t_1$

Referring to Fig. 3(a), in module A, $S_a$ conducts. Thus, the voltage across $N_{Pa}$ equals to the rectified line-in voltage $V_{in}$. The inductor current $i_{La}$ increases linearly, and $D_a$ is reverse-biased. In module B, $S_b$ is turned off. The voltage across $N_{Pa}$ is coupled to $N_{Pb}$. Hence, the voltage across $N_{Pb}$ is also $V_{in}$, and the dotted terminal is positive. $L_b$ stores energy as $L_a$ does. The inductor current $i_{Lb}$ increases linearly and flows into the nondotted terminal of $N_{Pb}$. By the coupling effect, this current flows into the dotted node of $N_{Pa}$. Since the voltage across $S_b$ is zero, $D_b$ is also reverse-biased. $C_o$ supplies the energy to the load. The constant turn-on time of $S_a$ is decided by the management of the controller depending on the rectified line-in voltage $V_{in}$. The inductor currents, $i_{La}$ and $i_{Lb}$, and the voltages across the switches, $v_{DSa}$ and $v_{DSb}$, can be expressed as follows:

$$i_{La}(t) = \frac{V_{in}}{L_a} (t - t_0) + i_{La}(t_0) \quad (1)$$

$$i_{Lb}(t) = \frac{V_{in}}{L_b} (t - t_0) + i_{Lb}(t_0) \quad (2)$$

$$v_{DSa}(t) = 0 \quad (3)$$

$$v_{DSb}(t) = 0. \quad (4)$$

The winding currents of $N_{Pa}$ and $N_{Pb}$, $i_{Pa}$ and $i_{Pb}$, are respectively

$$i_{Pa}(t) = i_{La}(t) + i_{Lb}(t) \quad (5)$$

$$i_{Pb}(t) = 0. \quad (6)$$
\[ i_{\text{L,b}}(t) = \frac{(V_{\text{in}} - V_o)}{L_b} (t - t_1) + i_{\text{L,b}}(t_1) \] (8)

\[ v_{\text{D,Sa}}(t) = V_o \] (9)

\[ v_{\text{D,SB}}(t) = V_o \] (10)

In addition, \( i_{\text{P,a}} \), \( i_{\text{P,b}} \), and the output diode currents, \( i_{\text{D,a}} \) and \( i_{\text{D,b}} \), are, respectively

\[ i_{\text{P,a}}(t) = i_{\text{L,a}}(t) \] (11)

\[ i_{\text{P,b}}(t) = i_{\text{L,b}}(t) \] (12)

\[ i_{\text{D,a}}(t) = i_{\text{L,a}}(t) \] (13)

\[ i_{\text{D,b}}(t) = i_{\text{L,b}}(t) \] (14)

**State 3: \( t_2 < t < t_3 \)**

As shown in Fig. 3(c), in module A, \( S_a \) keeps turned OFF. At \( t_2 \), \( D_a \) is turned OFF with ZCS since \( i_{\text{L,a}} \) decreases to zero naturally. Similarly, in module B, \( S_b \) is still turned OFF. \( D_b \) is turned OFF with ZCS at \( t_2 \) since \( i_{\text{L,b}} \) decreases to zero naturally, too. In this interval, \( C_o \) supplies the energy to the load. The voltage generated by the zero-crossing detector (ZCD) circuit decreases to the level which is preset by the controller. Then, this state ends and it enters the next half-switching cycle, of which the operating modes are similar to the aforementioned three states. In this state, \( i_{\text{L,a}}, i_{\text{L,b}}, v_{\text{D,Sa}}, \) and \( v_{\text{D,SB}} \) can be expressed as

\[ i_{\text{L,a}}(t) = \frac{(V_{\text{in}} - V_o)}{Z_a} \times \sin \omega_{oa}(t - t_2) \] (15)

\[ i_{\text{L,b}}(t) = \frac{(V_{\text{in}} - V_o)}{Z_b} \times \sin \omega_{ob}(t - t_2) \] (16)

\[ v_{\text{D,Sa}}(t) = V_{\text{in}} + (V_o - V_{\text{in}}) \times \cos \omega_{oa}(t - t_2) \] (17)

\[ v_{\text{D,SB}}(t) = V_{\text{in}} + (V_o - V_{\text{in}}) \times \cos \omega_{ob}(t - t_2) \] (18)

where \( Z_a, Z_b, \omega_{oa}, \) and \( \omega_{ob} \), are, respectively

\[ Z_a = \sqrt{\frac{(L_a//L_b)}{C_{\text{oss,a}}}} \] (19)

\[ Z_b = \sqrt{\frac{(L_a//L_b)}{C_{\text{oss,b}}}} \] (20)

\[ \omega_{oa} = \frac{1}{\sqrt{(L_a//L_b)C_{\text{oss,a}}}} \] (21)

\[ \omega_{ob} = \frac{1}{\sqrt{(L_a//L_b)C_{\text{oss,b}}}} \] (22)
In addition, $i_{Pa}$ and $i_{Pb}$ are

$$i_{Pa}(t) = i_{La}(t)$$  \hspace{1cm} (23)$$

$$i_{Pb}(t) = i_{Lb}(t).$$  \hspace{1cm} (24)

The ZCD circuit of the proposed topology adopts the UCC28060, an interleaving dual-phase transition-mode PFC controller of Texas Instruments [25], and the additional circuit shown in Fig. 4. Theoretically, the turn-on instants of the two switches are, respectively, decided by detecting the waveforms of $v_{DSa}$ and $v_{DSb}$ to check if a preset voltage level is touched while $v_{DSa}$ and $v_{DSb}$ drop from $V_o$. However, from Fig. 2, it can be seen that the waveforms of $v_{DSa}$ and $v_{DSb}$ are the same. Therefore, if the ZCD function of the UCC28060 is adopted directly, there will be an error situation of the synchronous conduction of the two switches, instead of the required push–pull operation. To solve this problem, an additional ZCD circuit is proposed and analyzed. The ZCD signal obtained from the ZCD circuit of the UCC28060 can effectively avoid the synchronous conduction of the two switches.

### III. Circuit Design Procedures

From the flux balance of $L_a$ or $L_b$ under the steady state, the transfer ratio of $V_o$ to $V_{in}$ can be obtained. For module A, $S_a$ conducts in state 1, of which the time interval is $DT_s$. The voltage across $L_a$ is $V_{in}$. $S_a$ turns off in state 2, of which the time interval is $t_{off}$, and the voltage across $L_a$ is $(V_{in} - V_o)$. Since $t_{qr}$, the time interval of state 3, occupies relatively 17.3 percent of a half-switching cycle, $t_{off}$ can, thus, be approximated as $(1/2 - D)T_s$. The flux balancing equation of $L_a$ is

$$V_{in} \times DT_s = (V_o - V_{in}) \times \left( 1 - 2D \right) T_s.$$  \hspace{1cm} (25)

The transfer ratio of $V_o$ to $V_{in}$ can be obtained as

$$\frac{V_o}{V_{in}} = \frac{1}{1 - 2D}.$$  \hspace{1cm} (26)

In addition, the maximum duty cycle $D_{max}$ can be obtained from (26)

$$D_{max} = \frac{V_o - \sqrt{2V_{in}V_{rms(min)}}}{2V_o}.$$  \hspace{1cm} (27)

where $V_{in}V_{rms(min)}$ is the minimum rms line voltage.

$L_a$ and $L_b$ are coupled in a magnetic core. Both the inductances and the numbers of windings are the same. Let the equivalent inductance ($L_a||L_b$) formed by the parallel connection of $L_a$ and $L_b$ be $L_m$

$$L_a = L_b = 2L_m.$$  \hspace{1cm} (28)

Then, the relationships among the equivalent peak current, $i_{Lm(peak)}$, for $L_m$ to completely release energy to the load, the peak current of $L_a$, the peak current of $L_b$, $i_{La(peak)}$, and $i_{Lb(peak)}$, can be obtained accordingly

$$i_{La(peak)} = i_{Lb(peak)} = \frac{1}{2} i_{Lm(peak)}.$$  \hspace{1cm} (29)

There are two equations relating to the peak inductor currents during state 1

$$V_{in} = L_a \frac{i_{La(peak)}}{DT_s}.$$  \hspace{1cm} (30)

$$V_{in} = L_b \frac{i_{Lb(peak)}}{DT_s}.$$  \hspace{1cm} (31)

From geometric analysis, the peak line current $\sqrt{2}I_{in,\text{rms}}$ is the average value of $i_{Lm(peak)}$.

$$\sqrt{2}I_{in,\text{rms}} = \frac{i_{Lm(peak)}}{2}.$$  \hspace{1cm} (32)

$$I_{in,\text{rms}} = \frac{P_o}{\eta V_{in,\text{rms}}}.$$  \hspace{1cm} (33)

where $P_o$ is the output power, and $\eta$ is the conversion efficiency.

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$L_m$ and $i_{L_m(\text{peak})}$ can thus be obtained from (28) to (33) as

$$L_m = \frac{\eta D V_{\text{in,rms}}^2}{2 P_o f_s}$$

(34)

$$i_{L_m(\text{peak})} = \frac{2\sqrt{2} P_o}{\eta V_{\text{in,rms}}}$$

(35)

where $V_{\text{in,rms}}$ is the rms line voltage and $f_s$ is the switching frequency.

Therefore, $L_a$ and $L_b$ are as follows:

$$L_a = L_b = 2 L_m = \frac{\eta D V_{\text{in,rms}}^2}{P_o f_s}.$$  

(36)

Since the proposed PFC is controlled with constant on-time and frequency modulation, the design criteria are considered under $V_{\text{in,rms(min)}}$ and the rated output power $P_o(\text{rated})$ to ensure the TM operations. Therefore, the selections of $L_a$ and $L_b$ are as follows:

$$L_a = L_b = \frac{\eta D_{\text{max}} V_{\text{in,rms(min)}}^2}{P_o(\text{rated}) f_s(\text{min})}.$$  

(37)

where $f_s(\text{min})$ is the minimum switching frequency. $N_{Pa}$ and $N_{Pb}$ can be calculated from Faraday’s law

$$N_{Pa} = N_{Pb} = \frac{\sqrt{2}V_{\text{rms(min)}} D_{\text{max}} \times 10^8}{A_e f_s(\text{min}) B_{\text{max}}}$$

where $B_{\text{max}}$ is the maximum flux density, and $A_e$ is the effective cross-sectional area of the magnetic core.

It needs careful design of the ZCD winding $N_{zcd}$ since the signal detected from $N_{zcd}$ is fed into the inverting input of the D flip-flop. The minimum high level of the ZCD signal should be larger than the minimum input high-voltage $V_{IH}$ of the inverting input of the D flip-flop to ensure the correct operation of the additional ZCD circuit.

$$N_{zcd} = \frac{N_{Pa} V_{IH}}{V_{o} - \sqrt{2}V_{\text{rms(max)}}}$$

(39)

where $V_{\text{in,rms(max)}}$ is the maximum rms line voltage.

In addition, the peak currents of the switches, $i_{Sa(\text{peak})}$ and $i_{Sb(\text{peak})}$, the peak currents of the output diodes, $i_{Da(\text{peak})}$ and $i_{Db(\text{peak})}$, the rms currents of the switches, $i_{Sa(\text{rms})}$ and $i_{Sb(\text{rms})}$, and the rms currents of the output diodes, $i_{Da(\text{rms})}$ and $i_{Db(\text{rms})}$ are expressed as follows:

$$i_{Sa(\text{peak})} = i_{Sb(\text{peak})} = i_{L_m(\text{peak})}$$

(40)

$$i_{Sa(\text{rms})} = i_{Sb(\text{rms})} \approx \frac{i_{Lm(\text{peak})}}{\sqrt{2}} \sqrt{\frac{D}{3}}$$

(41)

$$i_{Da(\text{peak})} = i_{Db(\text{peak})} = \frac{1}{2} i_{L_m(\text{peak})}$$

(42)

$$i_{Da(\text{rms})} = i_{Db(\text{rms})} = \frac{i_{Lm(\text{peak})}}{\sqrt{2}} \sqrt{1 - D/6}.$$  

(43)

Therefore, the current stresses of the switches and the output diodes can be obtained as

$$i_{Sa(\text{max})} = i_{Sb(\text{max})} = \frac{2\sqrt{2} P_o(\text{rated})}{\eta V_{\text{in,rms(min)}}}$$

(44)

As in a standard boost converter, the maximum voltage stresses of the switches and the output diodes are all equal to $V_o$.

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

At first, the proposed PFC is simulated by the SIMetrix/SIMPLIS software. The results under $V_{\text{in,rms}} = 110 \, V_{ac}$, $P_o = 100 \, W$, $f_s = 110 \, kHz$, and $D = 0.285$ are shown in Fig. 5. These simulation results are similar to the key waveforms shown in Fig. 2. Therefore, the feasibilities of the proposed PFC are preliminarily verified.

A prototype is implemented and tested with the following circuit specifications and components:

1) line voltage: $V_{\text{in,rms}} = 90 \, V_{ac} \sim 264 \, V_{ac}$
2) output dc voltage: $V_o = 380 \, V_{dc}$
3) rated output power: $P_o(\text{rated}) = 200 \, W$
4) maximum duty cycle: $D_{\text{max}} = 0.35$
5) minimum switching frequency: $f_s(\text{min}) = 40 \, kHz$
6) magnetic core: TDK PQ32/20
7) maximum flux density: $B_{\text{max}} = 2500 \, Gauss$
8) conversion efficiency: $\eta = 94\%$
9) winding turns: $N_{Pa} = 25$, $N_{Pb} = 25$, and $N_{zcd} = 4$
10) inductances: $L_a = L_b = 320 \, \mu H$
11) switches $S_a$ and $S_b$: Infineon 11N60C3
Fig. 6. Implemented schematics of the proposed PFC.

12) output diodes $D_a$ and $D_b$: Shindengen SF20L60U;
13) output capacitor $C_o$: 220 $\mu$F/450 V.

Fig. 6 shows the implemented schematics of the proposed PFC. Some specifications such as line voltage range, output dc voltage, rated output power, minimum switching frequency, maximum flux density, and conversion efficiency should be specified first for designing the proposed PFC. The related parameters are then substituted into the circuit design procedures to complete the design of the proposed PFC. The maximum duty cycle $D_{\text{max}}$ is calculated first from (27). From (37) and (38), inductances $L_a$ and $L_b$ as well as winding turns $N_{Pa}$ and $N_{Pb}$ can be decided. The equivalent inductance of the coupled inductor is measured as about 160 $\mu$H from either side winding. The inductance of $L_a$ or $L_b$ thus almost equals to 320 $\mu$H due to the same winding turns of $N_{Pa}$ and $N_{Pb}$, which are parallel wound in the same magnetic core. The input filtering capacitance $C_{\text{in}}$ is 1 $\mu$F. The inductor current sensing resistance $R_s$ is 5 m$\Omega$. The D flip-flops and NAND gates in the additional ZCD circuit utilize HEF4013 and HEF4011, respectively.

Figs. 7 and 8 show the waveforms of the additional ZCD circuit drawn in Fig. 3. The tested conditions are $V_{\text{in rms}} = 110$ V$_{ac}$ and $P_o = 200$ W ($v_{GSa}/v_{GSb}/ZCD_a/ZCD_b$: 10 V/div, Time: 4 $\mu$s/div).

Fig. 7. Measured waveforms of $v_{GSa}$, $v_{GSb}$, $ZCD_a$, and $ZCD_b$ under $V_{\text{in rms}} = 110$ V$_{ac}$ and $P_o = 200$ W ($v_{GSa}/v_{GSb}/ZCD_a/ZCD_b$: 10 V/div, Time: 4 $\mu$s/div).

Fig. 8. Measured waveforms of $v_{GSa}$, $v_{GSb}$, $ZCD_a$, and $ZCD_b$ under $V_{\text{in rms}} = 220$ V$_{ac}$ and $P_o = 200$ W ($v_{GSa}/v_{GSb}/ZCD_a/ZCD_b$: 10 V/div, Time: 2 $\mu$s/div).

Fig. 9. Measured waveforms of $v_{GSa}$, $v_{GSb}$, $i_{Pa}$, and $i_{Pb}$ under $V_{\text{in rms}} = 110$ V$_{ac}$ and $P_o = 200$ W ($v_{GSa}/v_{GSb}/i_{Pa}/i_{Pb}$: 20 V/div, 5 A/div, Time: 4 $\mu$s/div).

Fig. 10. Measured waveforms of $v_{GSa}$, $v_{GSb}$, $v_{DSa}$, and $v_{DSb}$ under $V_{\text{in rms}} = 110$ V$_{ac}$ and $P_o = 200$ W ($v_{GSa}/v_{GSb}/v_{DSa}/v_{DSb}$: 250 V/div, Time: 2 $\mu$s/div).

$V_{\text{in rms}} = 110$ V$_{ac}$, $P_o = 200$ W, and $V_{\text{in rms}} = 220$ V$_{ac}$, $P_o = 200$ W, respectively. In state 1, $ZCD_a$ changes its logic state from high to low, while $ZCD_b$ stays at its previous high-logic state. Hence, only $v_{GSa}$, the driving signal of $S_a$, changes its logic state from low to high and turns $S_a$ ON. $S_b$ keeps turned OFF. In contrast, in State 3, $ZCD_a$ changes its logic state from high to low, while $ZCD_b$ stays at its previous high-logic state. Hence, only $v_{GSb}$, the driving signal of $S_b$, changes its logic state from low to high and turns $S_b$ ON. $S_a$ keeps turned OFF. It is clearly seen that the
additional circuit can avoid the simultaneous conduction of the two switches.

Fig. 9 shows the waveforms of \(v_{GSA}, v_{GSB}, i_{p_a}, \) and \(i_{p_b}\). Fig. 10 shows the waveforms of \(v_{GSA}, v_{GSB}, v_{DSA}, \) and \(v_{DSB}\). All are measured under \(V_{in\_rms} = 110 \, V_{ac}\) and \(P_o = 200 \, W\). \(S_a\) conducts at \(t_o\) with QR valley switching when \(v_{DSA}\) drops to its first valley. Practically, due to the nonideal coupled inductor with leakage inductance and the unmatched \(L_a\) and \(L_b\), there exists a time interval during which the leakage inductor releases its energy before \(L_a\) and \(L_b\) start to store energy and \(i_{t_a}\) and \(i_{t_b}\), and thus \(i_{p_a}\) and \(i_{p_b}\), increase linearly. Therefore, the measured waveforms in this time interval are slightly different from the ideal theoretical waveforms in Fig. 2. At the same time, \(D_o\) and \(D_b\) are reverse-biased and cuts \(i_{Dp_a}\) and \(i_{Dp_b}\) are zero. When both switches are turned off at \(t_1\), \(D_o\) and \(D_b\) conduct to carry the continuous \(i_{t_a}\) and \(i_{t_b}\). \(L_a\) and \(L_b\) release energies to the load. When \(i_{t_a}\) and \(i_{t_b}\) linearly decreases to zero at \(t_2\), \(D_o\) and \(D_b\) turn off with ZCS. After that, \(L_a\) and \(C_{ossa}\), and \(L_b\) and \(C_{ossa}\) start to resonate. At \(t_3\), \(S_b\) is then turned on with QR valley-switching feature through the ZCD circuits. The next half-switching cycle begins. The circuit operations are similar to the aforementioned described ones during the previous half-switching cycle. From Fig. 9, duty cycles of \(S_a\) and \(S_b\) are almost matched, and the peak values of \(i_{p_a}\) and \(i_{p_b}\) are also nearly equal. Therefore, it is verified that the proposed topology is capable of sharing the input current and output current equally. For the proposed topology, two individual inductors \(L_a\) and \(L_b\) are coupled by the two windings wound in the same magnetic core.

At a glance, \(L_a\) and \(L_b\) seem to be the magnetizing inductances of the core in Fig. 3(a). However, if this is the case, then the output diode \(D_b\) will be cut off in state 2, which does not confirms to the experimental results. Therefore, \(L_a\) and \(L_b\) are individual inductors for each module. From Fig. 10, it can be seen that both \(S_a\) and \(S_b\) achieve QR valley switching. The turn-on switching loss of each switch can be expressed as

\[
P_{onj} = \left( \frac{1}{2} \times C_{ossa} \times v_{DSj}^2 \times f_s \right)
\]

where \(j = a \) or \(b\), \(T_{ij}\) is the rise time of \(S_j\). Substituting the related parameters, such as \(V_{in\_rms} = 110 \, V_{ac}\), \(P_o = 100 \, W\), \(f_s = 110 \, kHz\), and \(T_{r} = 5 \, ms\) into (46), the turn-on switching loss of one switch with QR valley-switching at \(v_{DS} \approx 20 \, V\) is about 16 mW. On the contrary, the turn-on switching loss with hard switching at \(v_{DS} = 380 \, V\) is about 588 mW. Therefore, the switching losses can still be reduced substantially.

Figs. 11 and 12 show the waveforms of line voltages and currents at \(P_o = 200 \, W\) with added \(L-C\) filter at the input side. The input PFs are 0.997 and 0.992 for \(V_{in\_rms} = 110 \, V_{ac}\) and \(V_{in\_rms} = 220 \, V_{ac}\), respectively. The efficiencies and THD values measured at 25%, 50%, 75%, and 100% loads for \(V_{in\_rms} = 110 \, V_{ac}\) and \(V_{in\_rms} = 220 \, V_{ac}\) are listed in Tables I and II. The average efficiencies for \(V_{in\_rms} = 110\) and 220 Vac are 95.92% and 96.26%, respectively. The PF values are all above 0.91. The lower efficiency under \(V_{in\_rms} = 220 \, V_{ac}\) and \(P_o = 50 \, W\) can be revealed through the power-loss analysis. The power-loss distributions of the proposed PFC under \(V_{in\_rms} = 220 \, V_{ac}\) and \(P_o = 50 \, W\) can be classified as follows.

1. MOSFET power losses, including conduction losses, turn-on losses, and turn-off losses;
2. output diode power losses, including conduction losses and turn-on losses;
3. power loss of the inductor current sensing resistor;
4. power loss of the bridge rectifier;

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**Fig. 11.** Measured waveforms of line voltage \(V_{ac}\) and current \(i_{ac}\) under \(V_{in\_rms} = 110 \, V_{ac}\) and \(P_o = 200 \, W\) \((v_{ac}: \) 100 V/div, \(i_{ac}: \) 2 A/div, Time: 4 ms/div).

**Fig. 12.** Measured waveforms of line voltage \(V_{ac}\) and current \(i_{ac}\) under \(V_{in\_rms} = 220 \, V_{ac}\) and \(P_o = 200 \, W\) \((v_{ac}: \) 200 V/div, \(i_{ac}: \) 1 A/div, Time: 4 ms/div).

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**TABLE I**

<table>
<thead>
<tr>
<th>(V_{ac})</th>
<th>25% (50 W)</th>
<th>50% (100 W)</th>
<th>75% (150 W)</th>
<th>100% (200 W)</th>
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<tr>
<td>Efficiency</td>
<td>96.17%</td>
<td>96.32%</td>
<td>96.17%</td>
<td></td>
</tr>
<tr>
<td>PF</td>
<td>0.983</td>
<td>0.992</td>
<td>0.995</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>15.43%</td>
<td>6.07%</td>
<td>4.21%</td>
<td>3.14%</td>
</tr>
</tbody>
</table>

**TABLE II**

<table>
<thead>
<tr>
<th>(V_{ac})</th>
<th>25% (50 W)</th>
<th>50% (100 W)</th>
<th>75% (150 W)</th>
<th>100% (200 W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>97.35%</td>
<td>97.4%</td>
<td>97.75%</td>
<td></td>
</tr>
<tr>
<td>PF</td>
<td>0.961</td>
<td>0.937</td>
<td>0.95</td>
<td>0.961</td>
</tr>
<tr>
<td>THD</td>
<td>23.92%</td>
<td>15.31%</td>
<td>10.25%</td>
<td>8.6%</td>
</tr>
</tbody>
</table>

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5) power losses of the coupled inductor, including core loss, gap loss, and copper losses.

Fig. 13 shows the power-loss distribution of the proposed PFC under $V_{\text{in rms}} = 220\,\text{V ac}$ and $P_o = 50\,\text{W}$. It can be seen that the turn-on losses of the switches and the output diodes dominate. Although the proposed PFC features QR valley switching, the voltage valley at $V_{\text{in rms}} = 220\,\text{V ac}$ is not as low as that at $V_{\text{in rms}} = 110\,\text{V ac}$. In addition, the proposed PFC is operated under TM control with a constant on time and variable switching frequencies. The switching frequency is quite high at light loads. Therefore, the high-switching frequency and the not-low-enough voltage valley become the main causes for a lower efficiency under $V_{\text{in rms}} = 220\,\text{V ac}$ and $P_o = 50\,\text{W}$.

V. COMPARISONS AMONG VARIOUS PFCs

The comparisons among the proposed PFC, a TM boost PFC, and an interleaved TM boost PFC are discussed according to the common and different parts.

The common parts:
1) All inductors operate in TM. In addition, all PFCs are controlled under constant on-time and frequency modulation.
2) After the inductor completely releases its energy to the load, the series resonant network formed by the inductor and the output capacitor of the switch starts to resonate. During the resonances, the switches are turned on with valley-switching to reduce the turn-on switching losses. In addition, the output diodes turn off with ZCS since their currents naturally decrease to zero. Therefore, the turn-off switching losses can be reduced.

The different parts are as follows:

Table III lists the key parameters of the three PFCs. Some major differences are described as follows.
1) From the transfer ratios of $V_o$ to $V_{\text{in}}$, it is observed that the duty cycle of the proposed PFC is half those of the other two topologies. This means that the inductor windings are also cut half. Although the proposed PFC needs two windings, the cut-in-half duty cycle reduces the diameters of the windings. Hence, the total inductor volume is much less than those of the other two PFCs. In addition, the conduction losses are decreased to improve the conversion efficiency.

2) Under the same specifications, the inductance of the proposed PFC is the smallest of all. This helps reducing the inductor size. Although both the interleaved TM boost PFC and the proposed PFC need two inductors, the latter features a reduced inductor size due to the coupling nature.

3) Although the peak inductor current of the proposed PFC, $i_L(\text{peak})_p$, is the same as that of a TM boost PFC, the total energy of the inductors stored during a switching cycle $W_{\text{in}}$ is twice that of the TM boost PFC. It means that the proposed PFC is more suitable for medium power level applications.

4) Concerning the switches of the voltage stresses of these three PFCs are equal to the output voltage. The peak current of the proposed PFC, $i_S(\text{peak})$, is the same as that of a TM boost PFC. However, the duty cycle of the proposed PFC is half that of the TM boost PFC. Therefore, the rms switch current of the proposed PFC $i_S(\text{rms})$, is less than that of a TM boost PFC. It represents that the conduction losses of the proposed PFC can be reduced.

5) Concerning the stresses of the output diodes, the voltage stresses of these three PFCs are equal to the output voltage. Both the interleaved TM boost PFC and the proposed PFC can equally distribute the output current. In addition, the peak diode current of the proposed PFC, $i_D(\text{peak})$, is half that of a TM boost PFC. The output diode current ripple of the proposed PFC is thus half that of a TM boost PFC, which is the same as the interleaved TM boost PFC. However, the output current ripple of the proposed PFC is as large as the TM boost PFC because of the in-phase output diode currents. Without considering the hold-up time requirement, the output capacitances of both the proposed PFC and the TM boost PFC are theoretically the same, which is bulkier than that of the interleaved TM boost PFC. From the experimental results with the same output capacitance 220 μF/450 V under $V_{\text{in rms}} = 110\,\text{V ac}$ and $P_o = 200\,\text{W}$, the output voltage ripple of both the proposed PFC and the TM boost PFC are about 7 V, while the one of the interleaved TM boost PFC reduces to 5 V.

6) For the same applications in medium power level, the push–pull QR boost PFC possesses the highest power density, while the efficiency of the interleaved TM boost PFC is lower than that of the proposed PFC.
is the best of all. It can be realized from the inductor losses first. The push–pull QR boost PFC incorporates two inductors into one magnetic core to reduce the circuit volume substantially without increasing the flux density, but the operating frequency of the core is double the switching frequency. Hence, the core loss of the push–pull QR boost PFC is approximately equal to that of an interleaved TM boost PFC. Even with reduced winding turns, the effective inductance $L_m$ of the push–pull QR boost PFC is one-fourth of that of an interleaved TM Boost PFC. If these two PFCs adopt the same ferrite core with the same size, the gap loss of the push–pull QR boost PFC must be higher than that of the interleaved TM boost PFC. Secondly, from the view of switching losses of the switches, all the operating frequencies are the same, but the peak switch currents of the push–pull QR boost PFC are larger than those of an interleaved TM boost PFC, which results in more turn-off switching losses.

7) Figs. 14 and 15 show the efficiency comparisons among various PFCs under $V_{in,\text{rms}} = 110$ V$_{ac}$ and $V_{in,\text{rms}} = 220$ V$_{ac}$, respectively. “Single” stands for a TM boost PFC, “Push–Pull” stands for the proposed PFC, and “Interleaved” stands for an interleaved TM boost PFC. All types of the bridge rectifier, switches, output diodes, output capacitor, and magnetic core are the same as shown in Fig. 6. However, the winding turns and inductances among these PFCs are different. Both the winding turns of a TM boost PFC and an interleaved TM boost PFC are 50 turns, which is double of the proposed PFC. The effective inductance $L_m$ of the proposed PFC is half of that of a TM boost PFC, and one fourth of that of an interleaved TM boost PFC. From the experimental results under $V_{in,\text{rms}} = 110$ V$_{ac}$ and $V_{in,\text{rms}} = 220$ V$_{ac}$, the efficiencies of the proposed PFC are higher than the ones of a TM boost PFC above $P_o = 100$ W and $P_o = 150$ W, respectively. This fact apparently verifies that the cut-in-half duty cycle of the proposed PFC reduces the conduction losses and copper losses at heavier loads. The poor light-load efficiencies of the proposed PFC are due to higher switching losses. Comparing with an interleaved TM boost PFC, the power density of the proposed PFC is higher by integrating two boost inductors into one magnetic core, but the penalty is efficiency decrease.

VI. CONCLUSION

The detailed analysis and design of the proposed push–pull QR boost PFC are presented in this paper. Simulation results verify its feasibility. A prototype is implemented with a universal line voltage, an output dc voltage of 380 V, and an output power of 200 W. The average efficiencies with 110- and 220-V$_{ac}$ input voltages are 95.92% and 96.26%, respectively. The measured PF values are all above 0.91. Finally, comparisons among a TM boost PFC, an interleaved TM boost PFC, and the proposed PFC are made for the same medium-power-level applications. From the experimental results, the efficiencies of the proposed PFC are higher than the ones of a TM boost PFC at heavier loads since the cut-in-half duty cycle reduces the conduction losses and copper losses. The overall features of the proposed PFC are the higher heavy-load efficiencies than the ones of a TM boost PFC, and the smallest inductor size of all.

REFERENCES


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