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Lossless passive snubber for half bridge interleaved flyback converter

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Abstract: Discontinues output current of regular flyback converter will cause several problems such as large volume of output capacitor and also high output voltage noise. Interleaved structure can reduce output current ripple and process more power compared with single-phase flyback converter. Normally, reducing the weight and size of a converter is an important goal while designing. An efficient way to reduce the size and weight of a converter and thus increasing power density is increasing switching frequency. However, in this way, switching losses increases. A half bridge interleaved flyback converter with clamp circuit is introduced and improved with a passive lossless snubber circuit. In this structure, the stored energy in parasitic elements is absorbed by passive snubber at turn off instant to provide soft switching condition for all semiconductor elements. The proposed snubber is load independent which is an important characteristic. In addition, a 500 W prototype converter is implemented which can improve the efficiency more than 6%.

1 Introduction

Flyback converter is a popular DC–DC topology which is used in many low-power applications, whereas for higher-power applications, interleaved flyback structure is a proper choice. Interleaved flyback converter has two major advantages in comparison to single switch flyback converter: (i) ability to process more power and (ii) lower-current ripple at output. Owing to these advantages, interleaved flyback topology is very popular and is applied in many applications such as light emitting diode drivers [1], photovoltaic systems [2], DC–DC converters [3–10], telecommunication industry [7] etc.

In recent years, many interleaved flyback topologies have been introduced. A problem which exists in all of the flyback type converters is the energy stored in the leakage inductance which leads to voltage spikes across power switch at turn off instant. Therefore a way to overcome this issue is very important and can increase the converter efficiency. In addition, switching losses is another parameter that is very important. Switching losses will reduce the efficiency, and therefore limits power conversion density. An efficient way to reduce the volume of a converter is increasing switching frequency. However, this will result in higher-switching losses. Therefore, for increasing switching frequency in order to reduce the volume of a converter, switching losses must be recovered. For this issue, active and passive soft switching methods can be applied. If zero current switching (ZCS) condition at turn off and zero-voltage switching (ZVS) condition at turn on instants are not required, passive techniques are preferred because of simplicity and robustness.

In [3], an interleaved flyback converter with cross-coupled inductor is introduced. Although the converter operates as an isolated buck-type converter, but the switch voltage stress is near twice input DC voltage.

Thus, in applications with high input voltage, selecting proper semiconductor devices for the converter is difficult. In addition, converter operates under hard switching condition, and thus to increase the efficiency of the converter, a lossless snubber circuit should be added. In [4], an interleaved flyback converter is introduced which uses coupled input series concept. In this converter, since the converter operates as a flyback-forward converter, at turn on instant a surge current passes through the converter switch. The only element that suppresses this current is transformer leakage inductance. Therefore to reduce this current, leakage inductance must be increased which causes the converter losses to increase. Also in [5], an interleaved flyback converter with zero-voltage transition is introduced. In this structure, ZVS condition in both turn off and turn on instants are provided without adding any auxiliary switch. However, the voltage across switches is not clamped, and thus the voltage stress of switches in this structure is larger than twice input DC voltage.

To reduce the current ripple in the input and output of a DC–DC converter, Lin *et al.* [6] proposes an interleaved flyback converter. In this converter, active clamp circuit is used to suppress the voltage stress of switches. However, the voltage stress of main switches is higher than input DC voltage. In addition, active clamp circuit increases complexity of the control circuit. In addition, recently multicell interleaved flyback converter is introduced, which is suitable for low input voltage high-power applications. However, to provide desired characteristics, high number of cells should be applied, and thus the volume and weight of these converters are high [8–10].

To overcome hard switching losses, many topologies have been proposed [11–29]. In [11–19], active auxiliary circuits are used to achieve this goal. Active techniques have their own advantages, but generally they cause the control circuit to become complex. Passive techniques, do not apply any extra switch [20–29]. Therefore these converters can be controlled similar to regular DC–DC converters. In [28], a passive snubber circuit is proposed which can be applied to an interleaved flyback converter. However, the voltage and current stress of switches are increased. Moreover, the leakage inductance of the transformer applied in the snubber circuit cause to create a ringing on the switch voltage. In addition, Li and Chung [29] introduce a passive snubber which can be used in a half bridge interleaved flyback converter. However, the number of elements of this snubber circuit is high, and thus this causes the power conversion density of converter to decrease.

So based on above discussion, to implement an interleaved flyback converter following points should be considered:

(1) Leakage inductance of converter transformer.
(2) Switching losses.
(3) Maximum switch voltage stress.
(4) Power conversion density.

In this paper, a half bridge interleaved flyback converter is introduced. The proposed converter can overcome above listed problems by using a simple passive snubber and clamp circuit. The passive snubber provides ZVS condition at turn off instant for converter switches. At turn on instant, transformer leakage inductance provides ZCS condition for the converter switches. In addition, by using this passive snubber, all the semiconductor elements are soft switched, and thus the reverse recovery current of rectifier diodes are reduced.

An interesting characteristic of the proposed passive snubber is its load independent operation. The required energy to provide soft switching condition is obtained from input source and load variations cannot influence the achieved soft switching condition. In addition, in high input voltage applications, using a clamp circuit is necessary. The proposed converter has a passive clamp circuit, which clamps the voltage across switches at turn off instant.

This paper is arranged in five sections. Section 2 explains converter operation. In Section 3, design procedure is described and to prove theoretical analysis, experimental results are presented in Section 4.

2 Proposed converter

Fig. 1 shows the proposed half bridge interleaved flyback converter with passive snubber and clamp circuits. This converter is composed of two single switch flyback converters. In this topology, input DC voltage is divided by two capacitors. Therefore input voltage for each flyback converter is $V_S/2$. To provide ZVS condition at turn off instant, a passive snubber is employed for each converter. The snubber circuit for upper converter is composed of C_{S_1}, L_{S_1}, D_{S_1} and D_{S_3} and for the bottom converter C_{S_2}, L_{S_2}, D_{S_2} and D_{S_4} are the snubber circuits. D_{C_1} and D_{C_2} are clamp diodes.

Since at continues conduction mode (CCM), the current injected to C_O is continues, in this section, converter operation is discussed in CCM mode. In addition, in order to describe the converter as simple as possible, it is assumed that the leakage inductance is much smaller than the magnetising inductance and all switches and diodes are ideal.

In each switching cycle, the proposed converter has 14 modes. Owing to the symmetrical operation of each converter cell, 7 operating modes are discussed. Fig. 2 shows the equivalent circuit for each converter operating mode. In this figure, the lines which transmit the current are shown as bold lines. Also in Fig. 2, transformers T1 and T2 are modelled by a leakage inductance (L_{lk_1} and L_{lk_2}), a magnetising inductance (L_{m_1} and L_{m_2}) and an

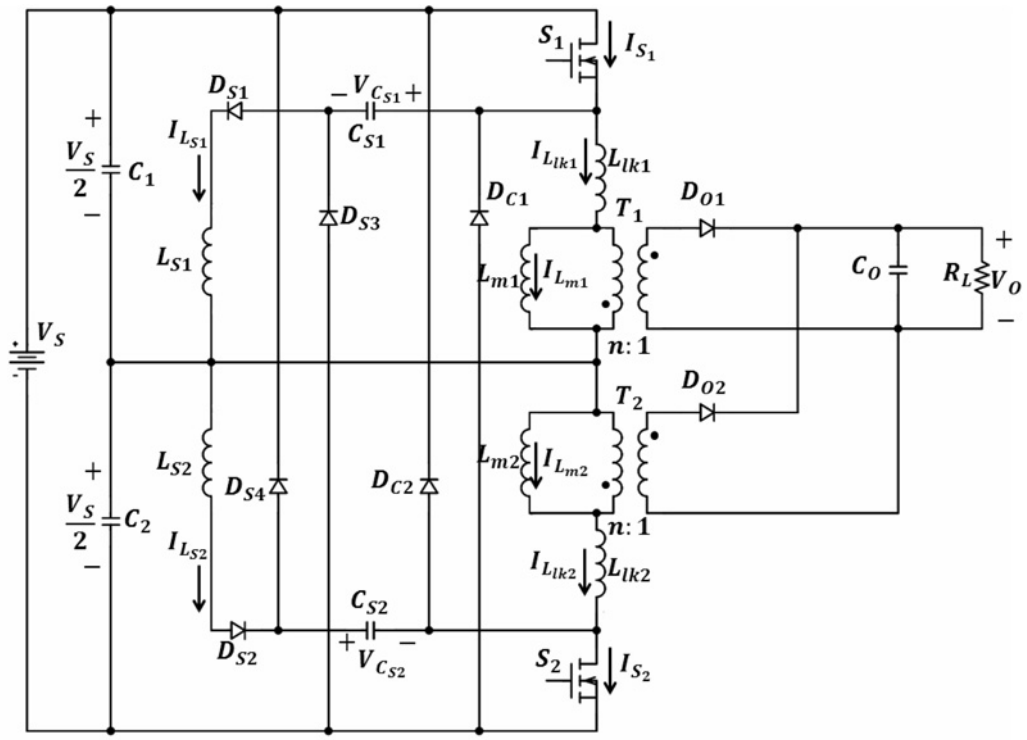

Fig. 1 *Proposed interleaved flyback converter*

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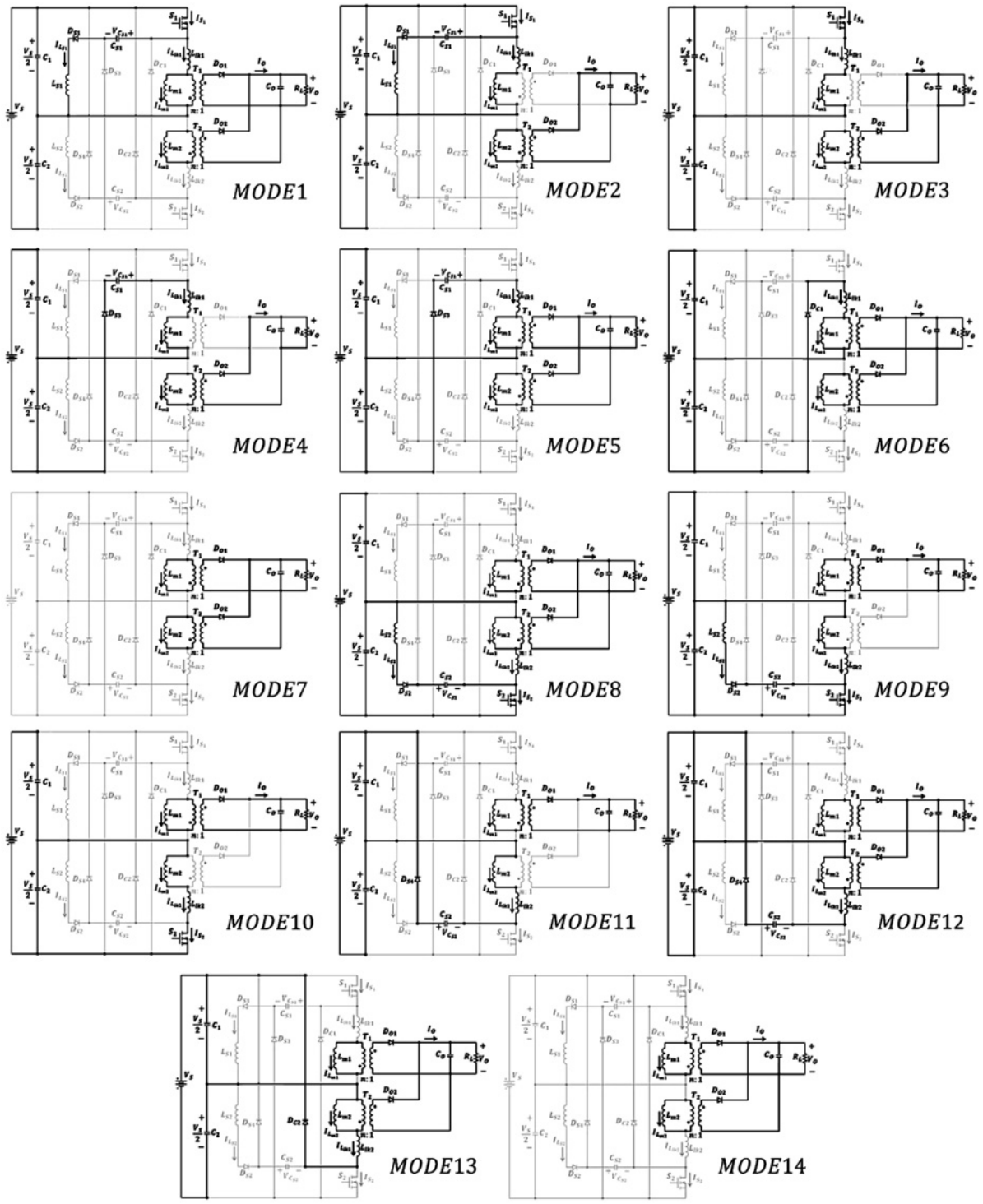

Fig. 2 *Equivalent circuit of each mode*

ideal transformer with n:1 turns ratio. Furthermore, in Fig. 3, important steady-state waveforms of the proposed converter are shown. The steady-state operation of converter in half of switching cycle is discussed as follows.

Mode 1: ($t_1 < t < t_2$)*:* It is assumed that before t_1, S_1 and S_2 are off, D_{O_1} and D_{O_2} are on and leakage inductances L_{lk_1} and L_{lk_2} currents are zero. Therefore L_{m_1} and L_{m_2} are discharging into output capacitance. On the other hand, in this situation, the power stored in L_{m_1} and L_{m_2} is transferred to the output.

At t_1, S_1 is turned on under ZCS condition because of L_{lk_1} and L_{S_1}. Thus in this interval, since the L_{lk_1} current is smaller than L_{m_1} current, D_{O_1} remains on. Therefore a voltage which is equal to $(V_S/2)+nV_O$ is placed across L_{lk_1} and the L_{lk_1} current increases linearly to $I_{L_{m_1}}$.

Also by turning S_1 on, D_{S_1} is turned on under ZCS and hence a resonance occurs between L_{S_1} and C_{S_1}. The important equations of this mode are

$$i_{L_{lk_1}}(t) = \frac{V_S/2 + nV_O}{L_{lk}}(t - t_1) \tag{1}$$

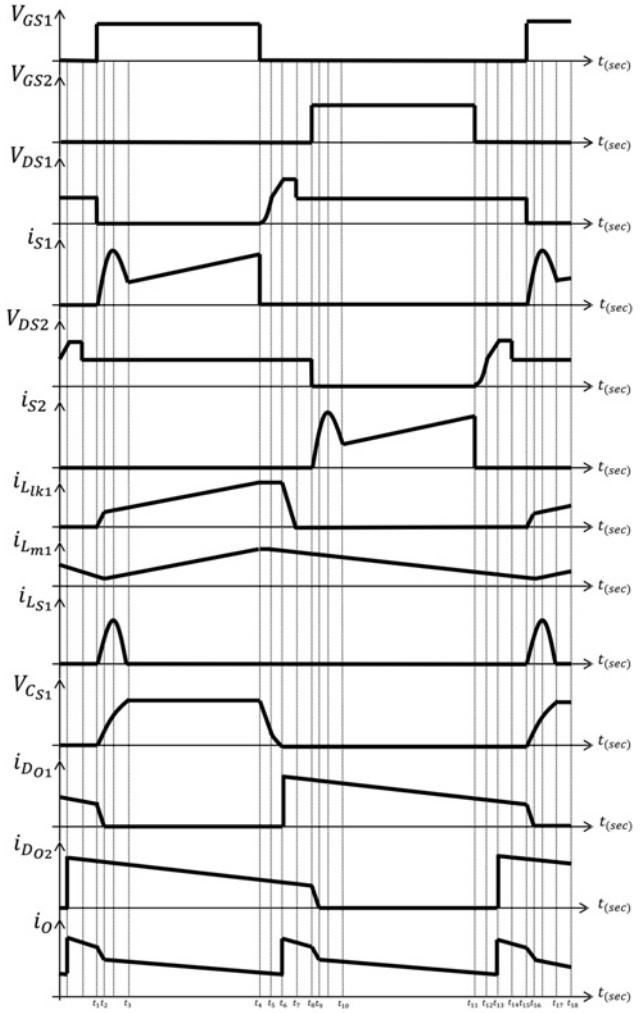

Fig. 3 *Steady-state waveforms*

$$i_{L_{m_1}}(t) = i_{L_{m_1}}(t_1) - \frac{nV_O}{L_m}(t - t_1) \tag{2}$$

$$V_{C_{S_1}}(t) = \frac{V_S}{2}(1 - \cos(\omega_0(t - t_1)) \tag{3}$$

$$i_{L_{S_1}}(t) = \frac{V_S}{2Z_0}\sin(\omega_0(t - t_1)) \tag{4}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_{S_1}C_{S_1}}} \tag{5}$$

$$Z_0 = \sqrt{\frac{L_{S_1}}{C_{S_1}}} \tag{6}$$

Mode 2: ($t_2 < t < t_3$)*:* When the current through L_{lk_1} becomes equal to $I_{L_{m_1}}$, D_{O_1} is turned off under ZCS, and thus a positive voltage is placed across L_{m_1} and it causes $I_{L_{m_1}}$ to increase linearly. In this mode, the resonance which started in mode1 will continue. This mode ends when $V_{C_{S_1}}$ reaches to V_S. The important equation of this mode is as follows

$$i_{L_{lk_1}}(t) = i_{L_{m_1}}(t) = i_{L_{lk_1}}(t_2) + \frac{V_S/2}{L_{m_1} + L_{lk_1}}(t - t_2) \tag{7}$$

Mode 3: ($t_3 < t < t_4$)*:* At t_3, $V_{C_{S_1}}$ reaches to V_S, and thus the resonance between L_{S_1} and C_{S_1} ends. In this mode, L_{m_1} is charged by input source. $I_{L_{m_1}}$ in this mode can be calculated from (7).

Mode 4: ($t_4 < t < t_5$)*:* At the beginning of this mode, S_1 is turned off and because of existence of L_{lk_1} and L_{m_1}, D_{S_3} turns on under ZVS. At previous modes, C_{S_1} was charged up to V_S. Thus, this charge causes S_1 to turn off under ZVS. Once D_{S_3} turns on, a resonance occurs between L_{m_1}, L_{lk_1} and C_{S_1}. Therefore during this resonance, C_{S_1} is discharged until its voltage reaches to $V_S/2 - nV_O[1 + (L_{lk}/L_m)]$. The important equations of this mode are as follows

$$i_{L_{lk_1}}(t) = i_{L_{m_1}}(t) = \frac{V_S}{2Z_1} \sin(\omega_1(t - t_4)) + i_{L_{m_1}}(t_4)\cos(\omega_1(t - t_4)) \tag{8}$$

$$V_{C_{S_1}}(t) = \frac{V_S}{2}[1 + \cos(\omega_1(t - t_4))] - Z_1 i_{L_{m_1}}(t_4)\sin(\omega_1(t - t_4)) \tag{9}$$

where

$$\omega_1 = \frac{1}{\sqrt{(L_{m_1} + L_{lk_1})C_{S_1}}} \tag{10}$$

$$Z_1 = \sqrt{\frac{L_{m_1} + L_{lk_1}}{C_{S_1}}} \tag{11}$$

Mode 5: ($t_5 < t < t_6$)*:* At t_5, D_{O_1} turns on under ZVS, and thus the stored energy in L_{m_1} is transferred to the output capacitor. In this mode, a new resonance occurs between L_{lk_1} and C_{S_1}. This resonance causes $V_{C_{S_1}}$ to reduce to zero. The important equations of this mode are as follows

$$i_{L_{lk_1}}(t) = i_{L_{lk}}(t_5)\cos(\omega_2(t - t_5)) - \frac{nV_O}{L_{m_1}\omega_2}\sin(\omega_2(t - t_5)) \tag{12}$$

$$i_{L_{m_1}}(t) = i_{L_{m_1}}(t_5) - \frac{nV_O}{L_{m_1}}(t - t_5) \tag{13}$$

$$V_{C_{S_1}}(t) = \left(\frac{V_S}{2} - nV_O\right) - Z_2 i_{L_{lk}}(t_5)\sin(\omega_2(t - t_5)) - \frac{L_{lk_1}}{L_{m_1}}nV_O\cos(\omega_2(t - t_5)) \tag{14}$$

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Table 1 Values of the converter elements

Converter elements	Values	Descriptions
L_{m_1} and L_{m_2}	250 μH	magnetising inductors
L_{lk_1} and L_{lk_2}	10 μH	leakage inductors
L_{S_1} and L_{S_2}	10 μH	snubber inductors
C_{S_1} and C_{S_2}	3 nF	snubber capacitors
C_1 and C_2	10 μF	divider capacitors
C_O	220 μF	output filter capacitors
n	2.9	turns ratio of the converter transformers

where

$$\omega_2 = \frac{1}{\sqrt{L_{lk_1} C_{S_1}}} \tag{15}$$

$$Z_2 = \sqrt{\frac{L_{lk_1}}{C_{S_1}}} \tag{16}$$

Mode 6: ($t_6 < t < t_7$)*:* At t_6, $V_{C_{S_1}}$ reduces to zero and D_{C_1} is turned on under ZVS, and thus the remained energy in L_{lk_1} is transferred to V_S. This mode ends when $I_{L_{lk_1}}$ reaches to zero. The important equations of this mode are

$$i_{L_{lk_1}}(t) = i_{L_{lk_1}}(t - t_6) - \frac{V_S/2}{L_{lk_1}}(t - t_6) \tag{17}$$

Mode 7: ($t_7 < t < t_8$)*:* In this mode, only the stored energy in L_{m_1} is transferred to the output. This mode ends by turning S_2 on.

3 Design procedure

To design the proposed converter, following assumptions can be considered:

(1) Leakage inductance is much smaller than magnetising inductance.
(2) All switches and diodes are ideal.

Based on the above considerations in CCM mode, duty cycle of converter can be achieved from following equation

$$D = \frac{2nV_O}{V_S + 2nV_O} \tag{18}$$

In addition, because of clamp diodes, the reflected voltage from secondary to primary side of transformer must be smaller than half of DC input voltage. Therefore the turns ratio of each transformer must be chosen from following equation

$$n < \frac{V_S}{2V_O} \tag{19}$$

where V_S is the minimum input DC voltage of the converter.

To design the converter, it can be noted that the main interleaved half bridge flyback converter can be designed just like any interleaved flyback type converter considering the effective input voltage of $V_S/2$. On the other hand, each flyback converter in the proposed converter must process half of the output power. Thus, this should be considered in designing the proposed converter. Therefore only the snubber circuit elements should be designed.

To provide ZVS condition at turn off instant, snubber capacitances must be calculated properly. These capacitors must limit the voltage across switch at turn off instant until the switch current reduces to zero. For this purpose, snubber capacitances (C_{S_1} and C_{S_2}) can be calculated from

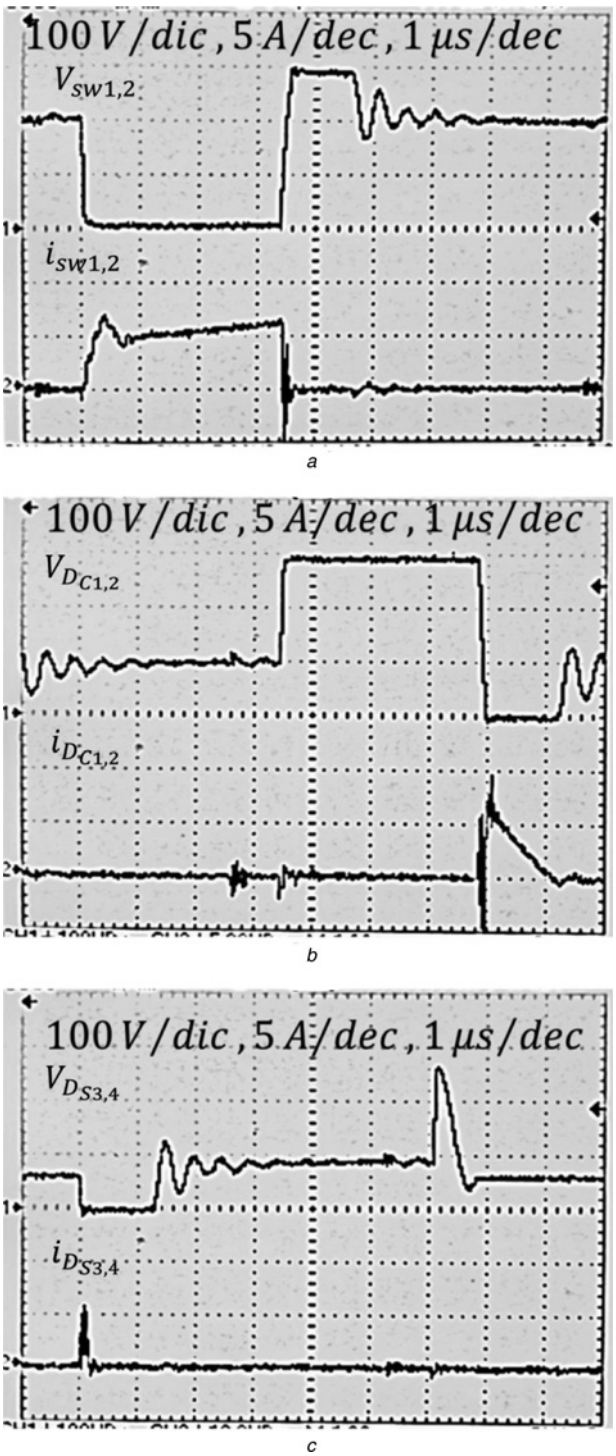

Fig. 4 *Experimental result*

a Drain–source voltage and current of switches
b Voltage and current of clamp diodes
c Voltage and current of D_{S_3} and D_{S_4}

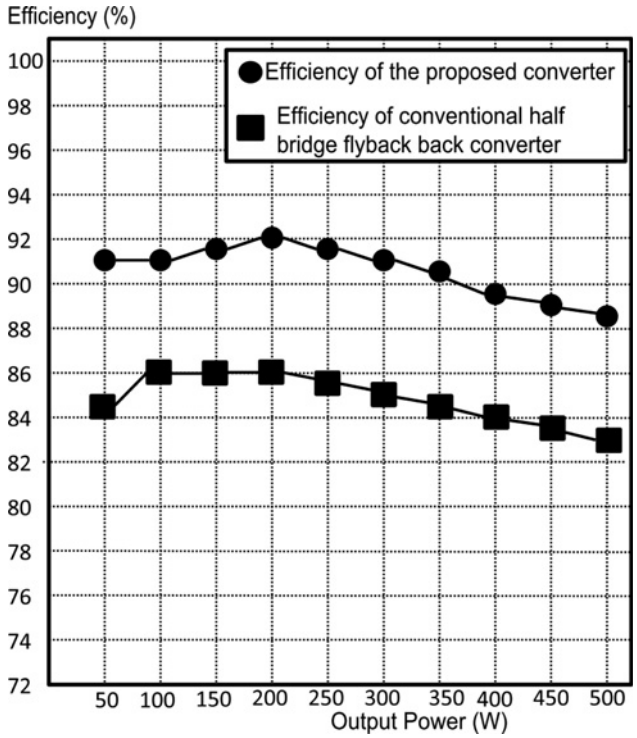

Fig. 5 *Efficiency diagram of the proposed converter against a conventional half bridge interleaved flyback converter*

following equation

$$C_{S_1} = C_{S_2} > \frac{\bar{I}_{sw} t_f}{V_S} \tag{20}$$

where t_f is the switch fall time, $\bar{I}_{sw}$ is the maximum switch current which occurs at turn off instant and can be calculated from (21)

$$\bar{I}_{sw} = \frac{\bar{P}_O}{\eta \underline{V_S} \bar{D}} \tag{21}$$

where $\bar{P}_O$ is converter maximum output power and η is the efficiency of the converter. Normally, η is chosen at the worst case, so 0.8 is a good choice for η in above equation. Also $\bar{D}$ can be calculated using (18).

To achieve ZCS condition at turn on instant, the value of leakage inductance is very important. To limit current increment rate at turn on instant, leakage inductances of converter (L_{lk_1} and L_{lk_2}) can be calculated from (22)

$$L_{lk_1} = L_{lk_2} > \frac{\bar{V}_S + 2nV_O}{2\Delta I} t_r \tag{22}$$

where $\bar{V}_S$ is the maximum input DC voltage, t_r is the switch rise time and ΔI is leakage inductance current variation. By considering ΔI equal to $\underline{P_O}/\bar{V}_S\underline{D}$, the ZCS condition at turn on instant can be achieved to provide ZCS condition at turn on instant.

4 Experimental results

Experimental results are presented in this section to justify the theoretical analysis. To prove soft switching condition can be achieved by the proposed converter, a 500 W prototype converter is implemented. The input DC voltage of the converter varies from 260 to 340 V and the output voltage of converter is 24 V and the switching frequency of the converter is 100 kHz. Also IRFP460 is used as converter switches, UF4004 as snubber and clamp diodes and BYV32 as rectifier diodes on the secondary side of the transformers. The other converter parameters are chosen based on the design considerations. Therefore the values of the converter elements can be observed in Table 1.

Fig. 4*a* illustrates the soft switching condition for converter switches. Also based on Figs. 4*b* and *c*, it is clear that soft switching conditions for snubber and clamp diodes are achieved.

As a comparison between proposed converter with a conventional half bridge interleaved flyback converter, Fig. 5 shows the efficiency diagram of the proposed converter along with efficiency diagram of conventional half bridge interleaved flyback converter, which is shown in Fig. 6. Passive snubber should be applied for hard switching converter. It is clear that the proposed converter can improve the efficiency because of recovered switching and snubber losses more than 6% at the maximum output power.

5 Conclusion

Normally single switch flyback converter is used in low-power applications. For high-power applications, interleaved flyback topologies are suggested. In power converters, the power conversion density is an important

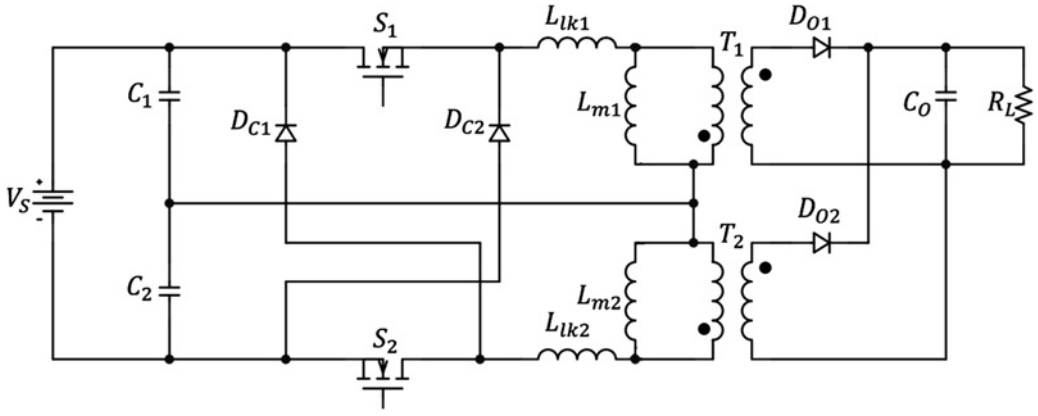

Fig. 6 *Conventional interleaved half bridge flyback converter*

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issue. The most efficient way to increase power conversion density is increasing switching frequency. Increasing switching frequency causes the switching losses to increase. Therefore to solve this problem, soft switching methods can be applied. In this paper, a half bridge interleaved flyback converter with a simple passive snubber and clamp circuits is introduced. This converter can be used in medium power applications. The snubber circuit applied in the proposed converter provides soft switching conditions for all of semiconductor elements. Therefore in this topology, switching losses are eliminated.

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