Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management

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***Abstract*—This paper discusses the theory and implementation of a class of distributed power converters for photovoltaic (PV) energy optimization. Resonant switched-capacitor converters are configured in parallel with strings of PV cells at the sub-module level to improve energy capture in the event of shading or mismatch. The converters operate in a parallel-ladder architecture, enforcing voltage ratios among strings of cells at terminals normally connected to bypass diodes. The balancing function extends from the sub-module level to the entire series string through a dual-core cable and connector. The parallel configuration allows converters to handle only mismatch power and turn off if there is no mismatch in the array. Measurement results demonstrate insertion loss below 0.1% and effective conversion efficiency above 99% for short-circuit current mismatch gradients up to 40%. The circuit implementation eliminates large power magnetic components, achieving a vertical footprint less than 6 mm. The merits of a resonant topology are compared to a switched-capacitor topology.**

***Index Terms*—Maximum power point tracking (MPPT), microinverter, resonant converter, solar energy, switched-capacitor.**

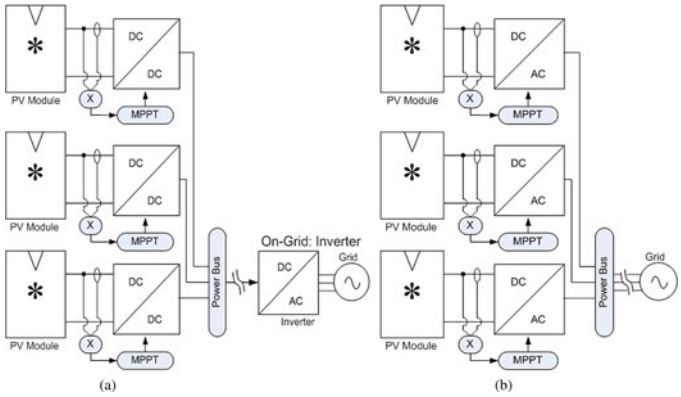

Fig. 1. First generation distributed power management solutions. (a) Distributed dc–dc converters. (b) Distributed dc/ac microinverters.

I. Introduction

SOLAR photovoltaic (PV) energy has gained increased prominence in recent years as a viable alternative to traditional carbon-producing sources of energy. To continue to drive PV energy toward cost parity with coal and other sources, there is a need to innovate in many areas including power electronics. The power management architecture can impact the viability of solar energy, increasing energy capture while reducing costs and solving painful integration issues [1]–[4].

The traditional PV power management architecture is based on a central inverter that manages one or more series-connected strings of PV panels [1]. The central inverter implements a maximum power point tracking (MPPT) algorithm that optimizes power flow from the solar array. Problems arise when there is mismatch among PV panels or strings of PV cells. Mismatch can arise from many sources including direct shading, dust, debris, cell aging, and factory mismatch [2]–[6]. In a string of panels, all PV cells are connected in series such that the current must be equal in all cells. With mismatch, the current in the series string is limited to the worst case cell in the string. In a traditional array, there may be ten or more panels connected in series which can result in hundreds of series-connected PV cells.

Bypass diodes placed in parallel with strings of cells in each PV module allow current to flow around underperforming strings of cells, but throw away energy produced by these cells and incur extra power loss in the diodes. This causes several problems: 1) power from underperforming cells can be lost even if it is only slightly lower than average, 2) the maximum power voltage V_{mpp} in strings of panels with bypass diodes "ON" will not match the V_{mpp} of other strings—resulting in power loss in all panels in the string, and 3) bypass diodes can cause discontinuities in the power–voltage curve for the array, complicating and potentially destabilizing the MPPT algorithm for the central inverter.

Recently, there have been efforts to decentralize power management for PV systems. First-generation distributed power management architectures include microinverters and per-module dc–dc converters [6]–[9]. As shown in Fig. 1(a), microinverters directly invert the dc power from the PV module into a parallel ac bus [8], [9]. Fig. 1(b) shows a distributed dc–dc converter system where each dc–dc converter optimizes a single solar module with a MPPT algorithm. Drawbacks to this approach include the extra cost and reliability overheads

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for the dc–dc converters, and lower peak power production due to the conversion efficiency penalty of the dc–dc converters, herein referred to as insertion loss. Here, insertion loss is defined as power loss overhead of distributed converters compared to the nominal (unshaded) power production of the PV array. For example, if PV modules are configured with dc–dc converters that have nominal conversion efficiency of 98%, insertion loss includes the conversion efficiency penalty of 2%. In some examples, dc–dc converters can operate in a pass-through or bypass mode when conversion ratio is exactly unity [6]. In this case, conversion efficiency of 99.5% or insertion loss of 0.5% has been reported. In practice, this approach requires the central inverter to operate the PV array with the exact voltage such that unity conversion ratio is achieved. This may be complicated for an array with multiple parallel strings of PV modules: strings may have different optimum pass-through voltages, especially if there is shading in the array.

This paper discusses an alternative architecture and class of distributed circuits for PV system optimization. In this study, distributed converters are configured in parallel with strings of PV cells at the sub-module level (in the junction box) to improve energy capture in the event of shading or mismatch. Similar to the work in [5], the parallel configuration allows converters to handle only mismatch power. Here, the embedded system allows converters to turn off if there is no mismatch in the array. Compared to traditional dc–dc converters, such as in [6] and [7], this can provide inherently higher conversion efficiency and near zero insertion loss, the latter being limited by the quiescent power of the embedded system. The converters operate in a parallel-ladder architecture, enforcing voltage ratios among strings of cells at terminals normally connected to bypass diodes. The ladder architecture has advantages compared to [5] with passive and active components exposed to only a fraction of total voltage stress. Similar to the discussion for switched-capacitor (SC) converters in [10]–[12], this can enable higher power density for the embedded converter. The architecture here also builds on the work in [13], which presents an SC ladder converter for battery equalization. In practice, low power design techniques can achieve insertion loss below 0.1%, providing effective conversion efficiency above 99.9% when mismatch among strings of cells is small. Importantly, effective conversion efficiency stays high, above 99% with mismatch up to 40% among adjacent strings of cells.

Compared to traditional buck–boost power point tracking solutions, the solution eliminates large power magnetic components, instead relying on high-power-density ceramic capacitors. This enables a vertical footprint of less than 6 mm which reduces air volume in packaging and thermal resistance to ambient, simplifying module co-integration. The mean-time-between-failures reliability metric is significantly higher due to component count reduction and low operational duty cycle because the converter can turn off when there is no mismatch. Configuration at the sub-module level enables recovery of mismatch loss at the string-of-cell level inside individual panels—this can impact intramodule shading effects such as dust rings on bottom or outer strings, spot mismatch such as debris or single-cell variation, or regular sub-module shading in tracking or fixed-tilt arrays.

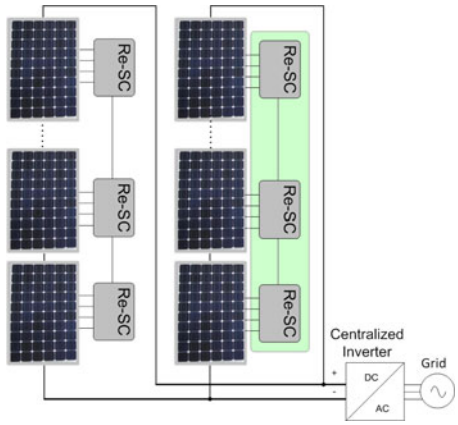

Fig. 2. Proposed resonant ladder converter architecture.

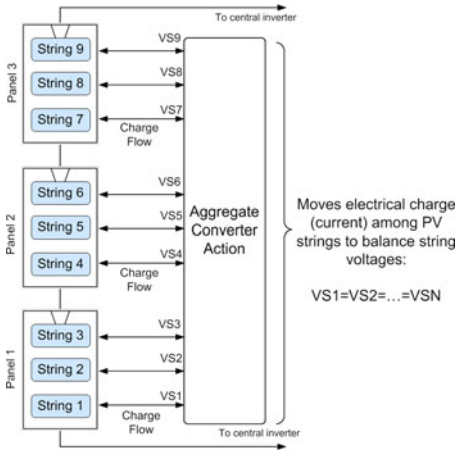

Fig. 3. Effective aggregate converter for one string of PV modules.

The architecture leverages the high conversion efficiency and reliability of state-of-the-art central inverters while providing a means to recover mismatch loss and implement other distributed control functions. As such it may be an attractive alternative in moderate to large-scale installations where microinverter cost and performance are less compelling.

The rest of this paper is organized as follows. Section II will discuss the proposed architecture. Sections III and IV will describe the theory and implementation of the proposed class of circuits. Section V and VI will discuss implementation and test results of the module-integrated circuit. Section VII will provide a conclusion.

II. Proposed Architecture

The proposed approach, shown in Figs. 2 and 3, is based on a distributed converter that is integrated in the junction box connector of each solar panel. In contrast with traditional dc–dc solutions that perform MPPT, the regulation objective of the proposed distributed converters is to enforce voltage ratios, not absolute voltages, among series-connected PV units. The converters interface across strings of cells in each panel in the traditional location of the bypass diodes, enabling better granularity of control than traditional dc–dc solutions. The distributed converters form an aggregate ladder converter that allows power

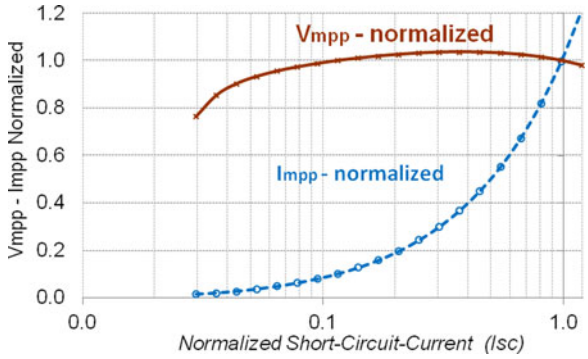

Fig. 4. Comparison of maximum power current and voltage (I_{mpp} and V_{mpp}) versus short-circuit current.

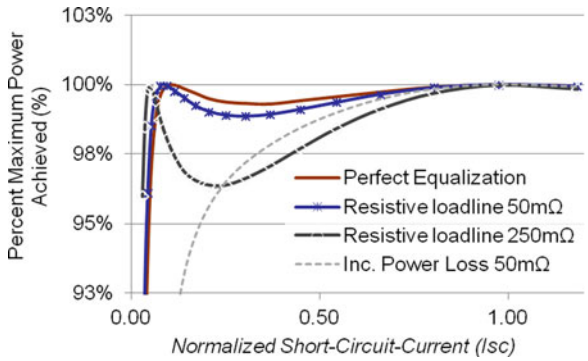

Fig. 5. Percent of maximum power achieved with voltage equalization strategy: compares perfect equalization and the case that the equalizer output follows a resistive loadline.

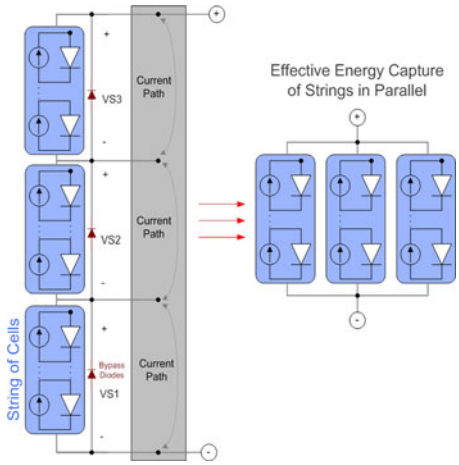

Fig. 6. Conversion process forms an effective parallelization of PV strings.

to flow in parallel with the series-connected PV modules. Fig. 3 shows the aggregate converter for one string of modules.

In typical PV modules, the voltage ratios of adjacent strings of cells are 1:1 assuming the strings have the same number of cells of the same technology. Since cell voltage is logarithmic with current to first order, maximum power voltage V_{mpp} is significantly less sensitive to mismatch than maximum power current I_{mpp}. Fig. 4 shows a comparison of the normalized I_{mpp} and V_{mpp} versus short-circuit current I_{SC} for a typical string of PV cells. I_{mpp} is linear with I_{SC} to first order, while V_{mpp} stays within a narrow range for nearly a decade of variation of I_{SC}. V_{mpp} is logarithmic with I_{SC} to first order, but has some higher order curvature due to series and shunt resistive effects. Maximum power voltage does have dependence on temperature such that thermal gradients can cause deviation from the 1:1 ratio, but the effect may only be a few percent even with thermal gradients up to 10–20 °C. Therefore, to first order, voltage equalization is effective to mitigate mismatch loss.

In the example discussed here, the converter enforces voltage ratios of 1:1 between adjacent strings of cells, which is equivalent to voltage equalization [13]. In the proposed system, the central inverter finds the maximum power voltage for the array, $V_{\mathrm{MP-Array}}$. In a system with N_P panels and N_S strings of cells per panel, each string of cells should operate at voltage $V_{\mathrm{String}} = V_{\mathrm{MP-Array}}/N_P \cdot N_S$. Since V_{mpp} varies less with mismatch, each string of cells should operate close to its maximum power point (MPP).

Fig. 5 shows the percent of maximum power achieved with the voltage equalization strategy. The *x*-axis represents the short-circuit current of a string of cells, normalized to the nominal I_{SC}. The curves are generated assuming the string of cells is connected in series with other strings that operate at nominal I_{SC}. Perfect equalization assumes all series strings operate at identical voltages. In this case, the underperforming string operates within 99% of its MPP for over a decade of variation of I_{SC}. The other curves represent the case that the voltage equalization circuit output follows a resistive loadline, providing less than ideal equalization. For output resistance of 50 mΩ and a nominal V_{mpp} around 15 V for the string, the string operates within 98.8% of MPP for a decade of I_{SC} variation. These curves reach 100% at two points because of the convex V_{mpp} curve in Fig. 4. It is important to note that this does not include the power loss in the converter and only indicates relative power production of the string of cells. The dashed curve in Fig. 5 includes the effect of power loss from the 50-mΩ loadline. Including resistive power loss in the balancing converter, the total power output is within 98% of MPP for I_{SC} variation of a factor of 2 and 90% for a decade of variation. In practice, current limits can be implemented to prevent reverse current flow into strings of PV cells which would occur in extreme shading situations as I_{SC} approaches zero.

Fig. 6 is a representation of a balancing converter operating in parallel with three strings of PV cells. With the converter operating to equalize voltage across strings of cells, the converter performs an effective parallelization of the strings. This effective parallelization provides a means to achieve the energy capture of strings connected in parallel while still achieving the higher voltage and lower copper interconnect of strings connected in series.

Major advantages of the architecture in Fig. 2 include that the each converter handles only the mismatch power, or difference in power between adjacent strings of cells. When there is no mismatch in the PV array, the converters can operate in a low-power mode or turn off. In contrast with the distributed dc–dc

architecture in Fig. 1(a), the full power flows through each dc–dc converter. This means that even if there is no shading or mismatch, the insertion loss of the dc–dc converters is $P_C/P_{\rm OUT}$ or $1-\eta_C$, where $P_{\rm OUT}$ is power output from the PV module, P_C is power loss in the converter, and η_c is the conversion efficiency of the converter. With a traditional dc–dc converter, insertion loss can be 2% or more depending on the performance of the converter and operating conditions of the panels. With the proposed architecture, insertion loss approaches the quiescent power consumption of the system that can be substantially less than 0.5% of generated PV power. For example, assuming hypothetical quiescent power is 1 W (to support instrumentation and communications functions in the embedded system), for a nominal 225-W panel, insertion loss is 0.44%. To highlight the efficiency advantage of the parallel configuration, assume the efficiency as measured only by the power flow into and out of the parallel converter is 90% in a module with two strings of cells and average power per string of 100 W (after mismatch is factored in). If the mismatch between adjacent strings is 10%, then the converter handles 10 W to balance power flow, with total power loss of 1 W. Effective conversion efficiency in this case is 99.5%.

III. SC Ladder Converter

SC circuits are effective for fixed-conversion-ratio applications as discussed in [10]–[14]. Fig. 7(a) shows a basic SC conversion cell with a 1:1 conversion ratio. Here, *VA* and *VB* are the voltages across input and output ports with power sources *V*1 and *V*2 that have series resistance R_S. C_X is a flying capacitance that transfers charge between *VA* and *VB*; $R_{\rm esr}$ represents the effective series resistance (ESR) of *Cx* and switch *S*1. In the slow switching limit, the configuration of C_X is modulated at a frequency $f_{\rm SW}$ that is less than *either* the self-resonant frequency or ESR time constant of the loops that contain C_{bp}, *S*1, $R_{\rm esr}$, and C_X [10], [11].

In phase 1, C_X is in parallel with *VA* storing charge $Q_A = C_X \cdot VA$. In phase 2, CX is in parallel with VB storing charge $Q_B = C_X \cdot VB$. If $VA > VB$, a net current will flow from *VA* to *VB*

$$I_{\rm DC} = \frac{VA - VB}{f_{\rm SW} \cdot C_X} \tag{1}$$

which can be modeled as an equivalent resistance

$$R_{\rm eff} = \frac{1}{f_{\rm SW} \cdot C_X}. \tag{2}$$

Here, $R_{\rm eff}$ is dependent only on switching frequency $f_{\rm SW}$, and flying capacitance C_X and has no dependence on $R_{\rm esr}$. The behavioral equivalent of the circuit in Fig. 7(a) is shown in Fig. 7(b), where $R_{\rm eff}$ is the same as in (2). Full details of the SC calculation and a comparison to the ReSC case are presented in [14].

The concept of Fig. 7(a) is extended to balance the string voltages of a PV module with the circuit represented in Fig. 8. The circuit shown in Fig. 8 implements an SC ladder converter with 1:1 conversion ratio, similar to the battery equalization circuit in [13]. Strings 1, 2, and 3 represent strings of PV cells in

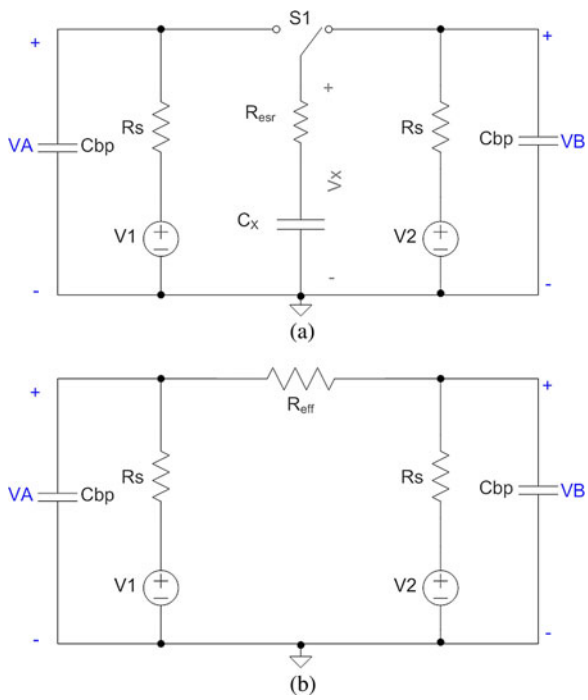

Fig. 7. (a) SC conversion cell. (b) Behavioral equivalent.

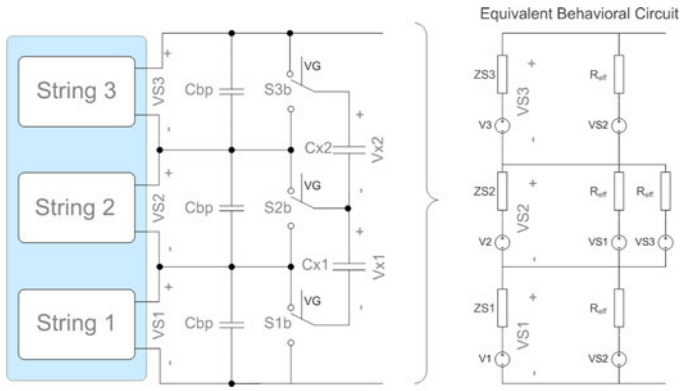

Fig. 8. SC ladder converter for balancing one PV module—similar to battery equalization circuit in [12].

a single module with voltages *VS*1, *VS*2, and *VS*3; C_{X1} and C_{X2} are flying capacitors; and *S*1*b*, *S*2*b*, and *S*3*b* represent single-pole double-throw switches. In the behavioral equivalent, *V*1, *V*2, and *V*3 represent the open-circuit voltage of the PV strings and *ZS*1, *ZS*2, and *ZS*3 represent the nonlinear output impedance of the strings. It can be shown that as $R_{\rm eff} \to 0$, or if $R_{\rm eff}$ is small compared to $|ZSi|$, then string voltages *VS*1, *VS*2, and *VS*3 will be forced substantially equal. It is important to note that $R_{\rm eff}$ is dually important parameter because it also captures power loss in the circuit—lower $R_{\rm eff}$ improves the effective conversion efficiency of the converter.

Limitations of the SC approach include an inherent tradeoff between switching and conduction losses. This tradeoff is inherent in (2) where it is shown that $R_{\rm eff}$ is inversely proportional to frequency. Reducing $R_{\rm eff}$ to achieve better equalization and higher power handling is at the expense of higher switching

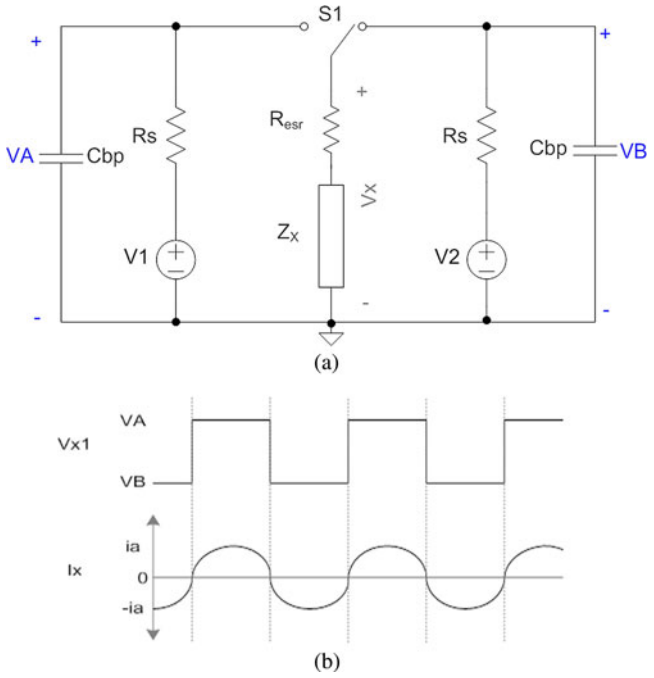

Fig. 9. (a) Resonant impedance conversion cell. (b) Current and voltage waveforms.

frequency. Another limitation is the fast switching limit (FSL) that is governed by *either* the ESR time constant or self-resonant frequency of the circuit. Onset of the FSL will enforce a minimum achievable $R_{\rm eff}$ that is dependent on $R_{\rm esr}$ [10]. Further issues include high current spikes in the SC circuit that can complicate electromagnetic compatibility [14].

IV. Resonant Ladder Converter

An extension of the SC ladder architecture uses resonant flying impedance Z_X in place of flying capacitance C_X from Fig. 7(a). In the primary example, Z_X consists of series-connected inductance L_X and capacitance C_X. As shown in Fig. 9(a), the circuit can be simplified to a 1:1 conversion cell similar to the SC equivalent. Here, L_X, C_X, and $S1$ form a switched series-resonant impedance [15]. $R_{\rm esr}$ and L_X lump in the series resistance and inductance in the loops that contain C_X and the C_{bp}. If the circuit is switched at the resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{L_X \cdot C_X}} \tag{3}$$

the voltage difference between *VA* and *VB* will appear as a square wave across the resonant impedance, as shown in Fig. 9(b). If the quality factor *Q* of the resonant loop is substantially higher than 1, then the current waveform in the series-resonant impedance is approximately sinusoidal at f_0.

The effective resistance $R_{\rm eff}$ of the conversion cell can be derived by calculating the average current transfer from *VA* to *VB*. Assuming a sinusoidal current waveform, the amplitude of the current waveform in Z_X is

$$ia = \frac{2/\pi(\Delta V)}{R_{\rm esr}} \tag{4}$$

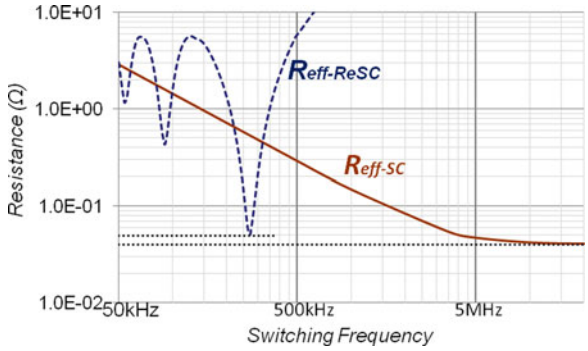

Fig. 10. Comparison of SC ($R_{\rm eff}$-SC) and resonant ($R_{\rm eff}$-ReSC) balancing cell performance metric.

where ΔV is the voltage difference *VA – VB* and $R_{\rm esr}$ is the ESR of the loop. The time-averaged current transferred by Z_X is

$$\overline{idc} = \frac{ia}{T_0}\int_0^{T_0/2} \sin\left(\frac{2\pi}{T_0}t\right) dt \tag{5}$$

where $T_0 = 1/f_0$ is the period of the switching cycle and $\overline{idc}$ is the average current flow from *VA* to *VB*. The result of (5) is

$$\overline{idc} = \frac{ia}{\pi} = \frac{2/\pi^2(\Delta V)}{R_0} \tag{6}$$

which implies that

$$R_{\rm eff} = R_{\rm esr}\frac{\pi^2}{2} \approx 5 \times R_{\rm esr}. \tag{7}$$

The result shown in (7) implies that the effective impedance of the resonant balancing circuit is only dependent on $R_{\rm esr}$ and has no dependence on frequency (given operation at f_0), or the individual component values that make up Z_X. A complete analysis of the "effective resistance" model and comparison of SC and ReSC architectures is presented in [14].

Fig. 10 compares the performance of the SC cell to the resonant impedance converter in Fig. 9(a). Both circuits use the same total capacitance and ESR. The dashed line labeled $R_{\rm eff\text{-}ReSC}$ represents $R_{\rm eff}$ for the resonant cell, while the solid line labeled $R_{\rm eff\text{-}SC}$ represents $R_{\rm eff}$ for the SC cell. The dashed lines at the bottom represent the asymptote for the minimum $R_{\rm eff}$ for each circuit. For the resonant cell, $R_{\rm eff\text{-}min}$ is given by (7) or $R_{\rm eff\text{-}min} \approx 5 \times R_{\rm esr}$. For the SC, the minimum $R_{\rm eff}$ achieved in the fast-switching limit is $R_{\rm eff\text{-}min} \approx 4 \times R_{\rm esr}$, consistent with [10] and [14].

The difference in $R_{\rm eff\text{-}min}$ can be explained by the shape of the current waveform—for the resonant cell, the current waveform is sinusoidal, as in Fig. 9(b), while in the FSL, the current waveform approaches a square wave. The advantage of the resonant cell is that it can achieve nearly the same $R_{\rm eff\text{-}min}$, but at a lower frequency that can be set by the choice of inductor and capacitor. The lower operating frequency reduces switching losses, improving conversion efficiency for the cell. In the design process, the center frequency and *Q* of the resonant network can be chosen independently by scaling the ratio of inductance and capacitance in $Q = 1/R_{\rm esr}\sqrt{Lx1/Cx1}$. It is generally

desirable to set Q greater than 1 but less than 10 to minimize stresses on the components and to provide sufficient bandwidth around the center frequency to tolerate some component variation and nonlinearity.

The multiple minima in the curve for $R_{\text{eff-ReSC}}$ are due to subharmonic operation of the converter at odd submultiples of the resonant frequency. The subharmonic minima provide an opportunity to further reduce switching losses at light loads. For example, the converter can operate at $f_0/3$, $f_0/5$, etc., to reduce switching losses when necessary [14]. As shown in Fig. 10, the subharmonic minima can provide lower R_{eff} than the SC circuit with the same net capacitance.

Another important consideration is the frequency dependence of R_{esr}. It is common for ESR to increase with frequency due to high-frequency loss mechanisms such as eddy currents. Some capacitor technologies also have increased ESR at lower frequencies. Ceramic capacitors with X7R dielectric are an example [16]. In this case, the operating frequency can be chosen to minimize R_{esr} and switching losses in the converter to maximize conversion efficiency.

It is possible to improve the performance of the resonant balancing cell toward the limiting case of the FSL for the SC cell. As mentioned previously with Z_X operating at a single fundamental frequency, the limit is $R_{\text{eff-min}} = R_{\text{esr}}\frac{\pi^2}{2} \approx 5 \times R_{\text{esr}}$, where in the FSL, the limit is $R_{\text{eff-min}} = 4 \times R_{\text{esr}}$. By shaping the current waveform that flows in Z_X closer to an ideal square wave, efficiency can be improved. This is similar to the approach with current mode class-D and inverse class F ($F^{-}1$) power amplifiers [17], [18].

As shown in Fig. 11, by modifying Z_X to resonate at increasing odd harmonics of f_0, the current waveform better approximates a square wave. Fig. 12 shows simulation results that capture $R_{\text{eff-min}}$ for the cases of Z_X including the fundamental, shown in Fig. 11(a), and third and fifth harmonic shaping of the current waveform, shown in Fig. 11(b). In each case, $R_{\text{esr}} = 10\,\text{m}\Omega$. As expected, $R_{\text{eff-min}}$ approaches the limit of 40 mΩ when higher harmonics are included. This approach may be practical in some cases to optimize the performance of the converter. In other cases, it may introduce sufficient extra ESR in the harmonic networks that performance gains are not significant. Fig. 12 models the scenario that the ESR from switches dominates. In many cases, the ESR of the passive elements are on the order of the ESR of the switches which may reduce the benefit of the topologies in Fig. 11(b).

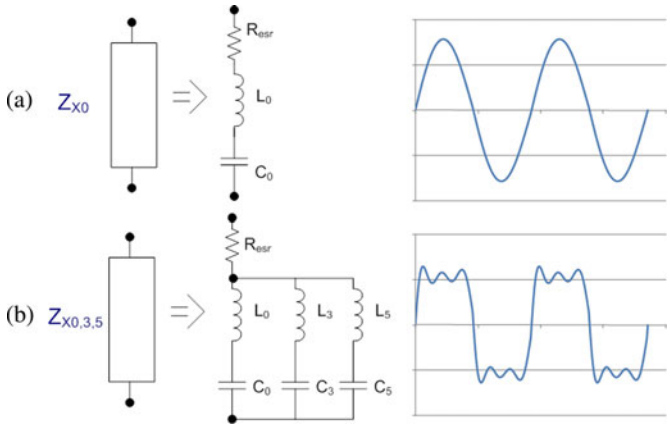

Fig. 11. Possible resonant impedance, Z_X, with fundamental, third harmonic, and fifth harmonic current waveform shaping.

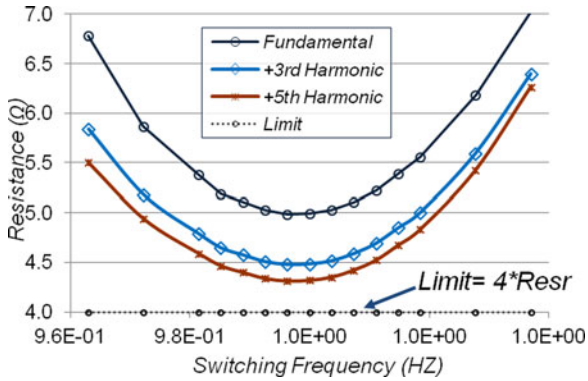

Fig. 12. Comparison of minimum R_{eff} for higher harmonic extensions of Z_X.

V. Circuit Implementation

Fig. 13 shows the top-level schematic representation of the proposed converter configured with a single PV panel. Also shown is the connectivity among the panel, voltage balancing circuit, and output terminals. To extend the balancing function across a string of panels, an extra stage is added to the circuit. In this case, string-3 is balanced with string-1 of the adjacent panel. Two additional terminals are required to provide both positive and negative voltages of string-1 of the adjacent panel. The terminals out of the package are the conventional positive and negative terminals of the PV panel (TB and TA), positive

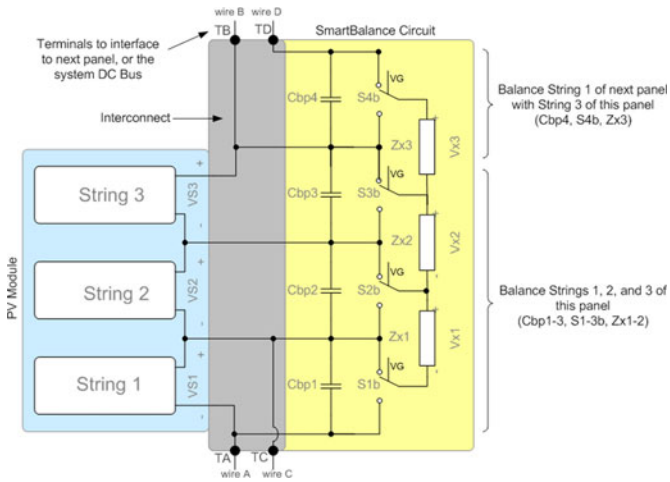

Fig. 13. Distributed converter circuit architecture.

voltage of string-1 of the panel (TC), and a terminal to accept the positive voltage of string-1 of the adjacent panel (TD). TA and TC can be housed in the same connector out of the package or junction box.

Fig. 14 shows the printed circuit board (PCB) implementation for the converter. Here, the terminals that connect to the PV module are shown on the top of the board. The output terminals,

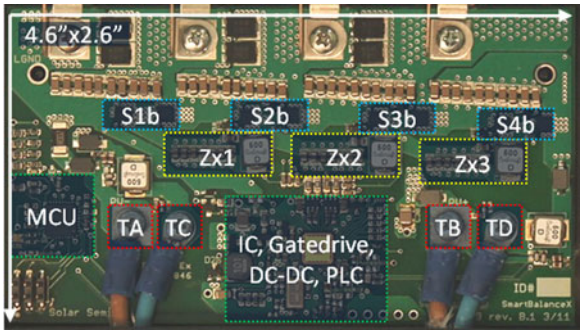

Fig. 14. PCB implementation.

TA-TD from Fig. 13, are indicated as labeled. These terminals connect between panels through a custom dual-conductor cable. The PCB includes the resonant power converter, local power management, sensing and instrumentation for panel voltage, current, and temperature, and a custom power-line communication circuit. The PCB includes a custom integrated circuit (IC) designed in a high-voltage 0.35-μm CMOS process with a 90-V LDMOS option. The 90-V process was required to support PV panels with open-circuit voltage up to 60 V, leaving some margin for device breakdown. The custom IC includes gate drivers for the resonant ladder converter, a local dc–dc converter and linear regulator, power-line communications transceivers, a crystal oscillator, a current sense amplifier, and other instrumentation functions. More details of the IC implementation are discussed in [19].

The gate drive for the ladder converter requires special attention to maximize performance and prevent problems. N-channel power semiconductors were used to implement double-pole switching action. As shown in Fig. 15, *M*1–*M*6 are N-channel power semiconductors and *M*7–*M*10 are clamping devices. Here, all switches but *M*1 require a floating driver referenced to the source terminal of the device. The on-chip driver creates a drive signal *VG*1,3,5 that is referenced to *V*0 to control *M*1, *M*3, and *M*5. The signal *VG*2,4,6 is referenced to the first stage switching node, *VSW*0, to control *M*2, *M*4, and *M*6. The power driver stage couples through capacitors to floating power switches.

The clamping devices set the "OFF" voltage for the floating power devices. In phase 1, when *M*1, *M*3, and *M*5 are "ON," *M*8 and *M*10 turn ON, connecting nodes *G*4 and *G*6 to nodes *V*1 and *V*2, respectively. In phase 2, when *M*2, *M*4, and *M*6 turn ON, *M*7 and *M*9 turn ON, connecting nodes *G*3 and *G*5 to nodes *V*1 and *V*2 respectively. Since each clamping device is controlled by the gate signal of the switch below it (in voltage), this helps to prevent shoot through current, even if there are transients on the gate signals or *V*0–*V*3 terminals.

Also, the clamping devices can establish the "OFF" voltage for the floating switches within one clock cycle—reducing the time for the switching waveform common mode to reach steady state and reducing power loss during startup. A further point to note is that some extra flying capacitance (not visible in Figs. 13 and 15) is placed in parallel with flying impedances, *Zxi* to reduce the loop area from the output of the floating gate driver back to its ground reference. This reduces inductance in series with the floating switches.

VI. Test Results

The circuit shown in Fig. 14 was tested in the laboratory with a power supply, electronic load, and an Agilent 34970A datalogger to collect current and voltage data. Current measurements were done with calibrated shunt resistors and the 34970A. An on-board microcontroller unit controls communication and system function including the switching frequency of the power converter. Fig. 16 shows measured results for effective resistance versus frequency and compares results to theory for the SC version with the same total capacitance. Flying impedance Z_X is implemented with multiple 1-μF ceramic capacitors off-chip that resonates with 50-nH total loop inductance, forming a 270-kHz resonant impedance.

Total $R_{\rm esr}$ is estimated at $\sim$11 mΩ including power semiconductors, capacitors, inductor, and board interconnect. Minimum effective resistance $R_{\rm eff\text{-}min}$ was measured at approximately 66.5 mΩ in the fundamental switching mode. This was slightly higher than the estimated value of $\sim$55 mΩ, as given by (7) and the estimated 11 mΩ $R_{\rm esr}$. Some deviation from theory is explained by finite rise time of the gate drive signals, high-frequency losses in board interconnect, and variation in component ESR. Measured third and fifth subharmonic minima, used for light-load operation, achieve $R_{\rm eff\text{-}min}$ of 0.52 and 1.33 Ω, but with switching losses scaled by one-third and one-fifth, respectively.

Fig. 17 shows effective conversion efficiency for a single module-integrated converter with a forced mismatch power gradient. The mismatch gradient is generated with a power supply simulating a three-string 225-W solar module and an electronic load. Here, the *x*-axis represents a linear gradient mismatch of short-circuit current available from three strings of PV cells in a single 225-W panel. Gradient mismatch is defined as $I_{{\rm SC}-i} - I_{{\rm SC}-j}/\overline{I_{\rm SC}}$, where $I_{{\rm SC}-i}$ and $I_{{\rm SC}-j}$ are short-circuit currents available from adjacent strings *i* and *j*, and $\overline{I_{\rm SC}}$ is average short-circuit current. The mismatch gradient and total power derived are measured with the 34970A datalogger with calibrated current shunts. Conversion efficiency is defined in the conventional sense as $\eta_C = \frac{P_{\rm out}-P_c}{P_{\rm out}}$, where $P_{\rm out}$ is total power output from the PV module and P_c is the power loss in the converter, including quiescent current for all embedded electronics.

As shown in Fig. 17, insertion loss was measured below 0.06% with panel mismatch at 0%. This measurement was consistent across 20 separate boards that used ICs built from four different reticles in a single wafer lot. Insertion loss was dominated by quiescent power for the embedded system which was between 50 and 90 mW for instrumentation, communication, and other functions. This leaves substantial room for improvement in future implementations. In the fundamental mode, effective conversion efficiency stayed above 99% for gradient mismatch up to 40%. At light mismatch, the converter can shift into subharmonic operation, switching at f_o/3 and f_o/5. To achieve maximum conversion efficiency, it makes sense to operate at

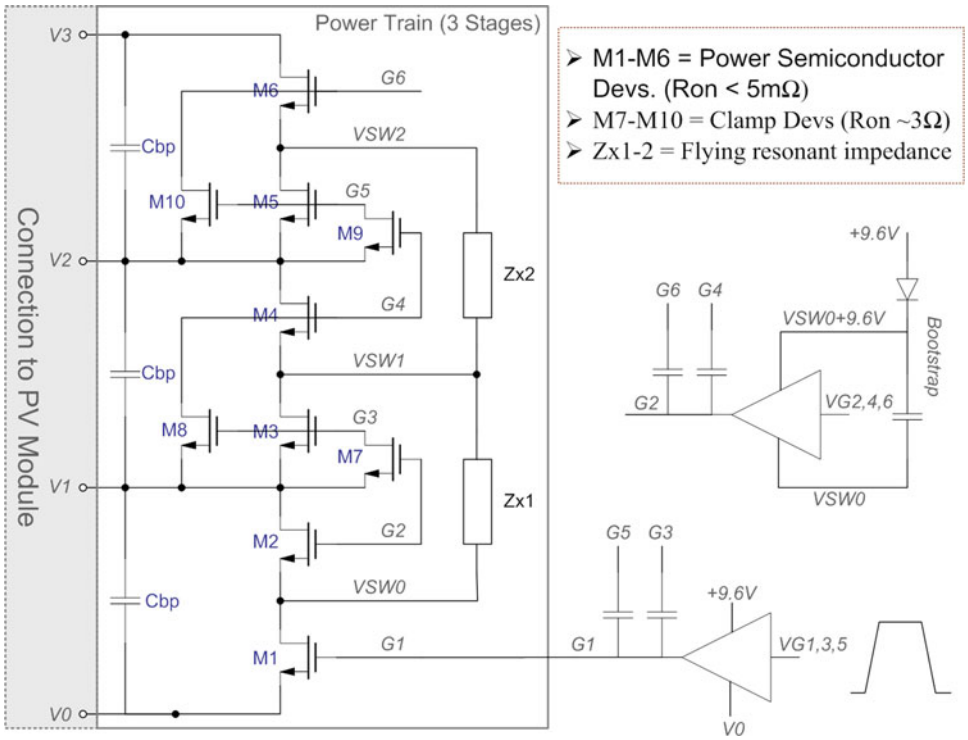

Fig. 15. Ladder converter gate-drive circuit.

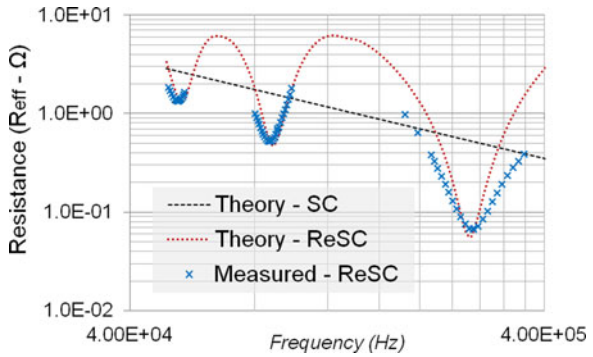

Fig. 16. Effective resistance R_{eff} plotted versus frequency.

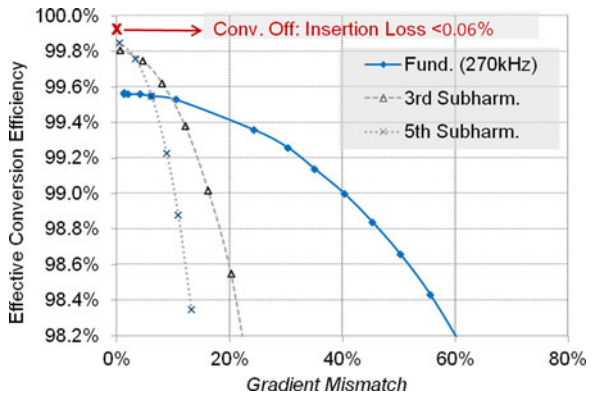

Fig. 17. Effective conversion efficiency versus gradient mismatch with a laboratory solar panel simulator.

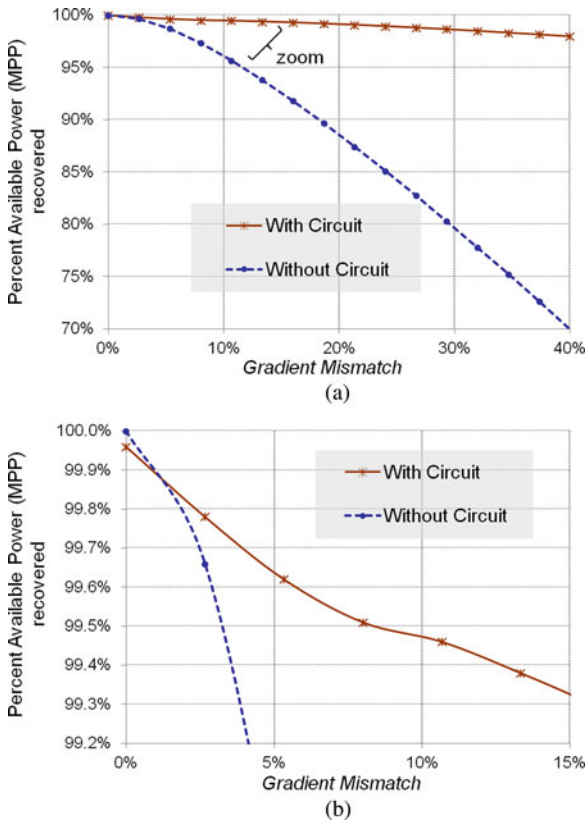

Fig. 18. (a) Percent available power recovered versus gradient mismatch. (b) Zoom-view of Fig 18(a) at low gradient mismatch level.

Fig. 19. 5.4-kW field test setup: 12 panels each in control string and test string.

Fig. 20. Example shading scenario: Half of two cells in 4 of 12 panels.

$f_o/5$ for gradient mismatch less than 4% and $f_o/3$ for mismatch less than 10%.

Fig. 18(a) and (b) shows the percent of available power recovered versus the same gradient mismatch profile in Fig. 17. Here, percent available power recovered is the maximum power output of the solar module divided by the sum of individual MPPs of the three strings. The measurement captures both the *power point tracking ratio* of the proposed solution and the *conversion efficiency* penalty. The two curves show the performance with and without the circuit present in the system. Importantly, the circuit enables significantly higher energy capture than the case without the circuit. For gradient mismatch up to 40%, the circuit enables capture of over 98% of available energy. Switching among the various modes of operation, the circuit achieves higher energy capture in light mismatch scenarios as well. The breakeven point, where the converter produces more energy than it consumes, occurs at a gradient mismatch between 1% and 2%, which is on the order of factory mismatch levels [3]. It should be noted that the case without the circuit is equivalent to a per-module power point tracking converter (such as a microinverter) because the mismatch gradient is across submodule strings. Also, while Fig. 18 is for a single PV module, the proposed circuit extends to multiple PV modules in series, enabling advantages for large strings of modules.

Figs. 19 and 20 show a field test setup for the proposed converter. Two identical strings of panels are installed in a ground-mount setup with total rated power of 5.4 kW. Each string has an identical SMA 3-kW inverter. There is no direct shading at the site other than horizon effects at sunrise and sunset. Data were measured with the 34970A datalogger and calibrated current shunts to ensure measurement accuracy better than 1%.

TABLE I
COMPARISON OF INSTANTANEOUS POWER: WITH AND WITHOUT CONVERTERS

	Unshaded	Shaded: Fig. 20
Power-Control	2.040kW	1.620kW
Power-Test	2.032kW	2.070kW
Power Gain	-0.40%	27.7%

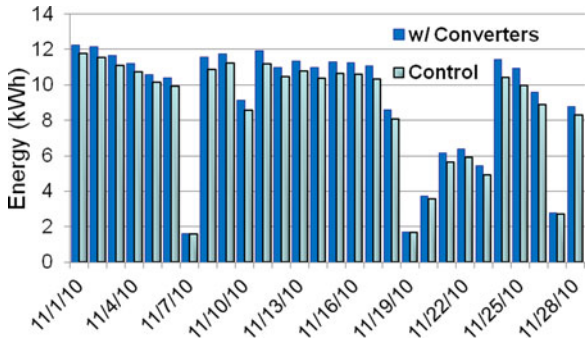

Fig. 21. Daily energy log for PV system in Fig. 19 for the month of November 2010.

Table I shows the instantaneous power of the control and test strings in two scenarios: unshaded as shown in Fig. 19 and shaded in the configuration of Fig. 20. In the unshaded scenario, the array with the proposed converters operates with around 8 W less power than the control string. This can be partly attributed to the quiescent power of the converters and confirms the nameplate matching of the two arrays is better than 1%. The scenario in Fig. 20 involves shading two cells in 4 of the 12 modules in the string. In this case, the string with the proposed converters provides around 450 W or 27.7% more power to the grid.

Fig. 21 shows the daily energy provided to the grid as logged by the two inverters in the system for the month of November 2010. While there is no direct shading in the array (the horizon is unobstructed), the system with the proposed converters achieved more power on average than the control string. For the month of November, the net energy benefit for the proposed approach was around 6%. The mismatch sources that result in this benefit have yet to be determined but it is expected to be related to cell/module aging combined with dust and debris accumulation.

VII. CONCLUSION

An architecture and circuit implementation for distributed sub-module PV energy optimization has been presented. The converter was based on a core resonant SC converter that enforces set voltage ratios across strings of PV cells at the submodule level. The parallel architecture enables near zero insertion loss and inherently higher conversion efficiency compared to traditional dc–dc MPPT solutions. The converter handles only mismatch power among adjacent strings of cells and can

turn off if there is no mismatch, providing reliability benefits of lower average power handling and lower operational duty cycle. A vertical footprint less than 6 mm due to elimination of large power magnetic components reduces air volume in packaging and simplifies module co-integration. Insertion loss was consistently measured below 0.1% for a number of parts, and conversion efficiency was above 99% for gradient mismatch above 40%. The converter and voltage equalization strategy was shown to recover over 98% of available energy for gradient mismatch up to 40% including power point tracking ratio and converter power consumption.

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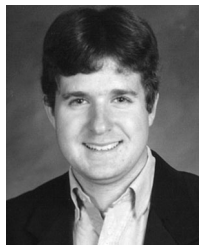

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