Hysteresis Current Control for Multilevel Converter in Parallel-Form Switch-Linear Hybrid Envelope Tracking Power Supply

Yazhou Wang, Xinbo Ruan, *Fellow, IEEE*, Yang Leng, Ying Li

***Abstract* — Parallel-form switch-linear hybrid (SLH) envelope tracking (ET) power supply is constituted by a linear amplifier and a switched-mode converter connected in parallel. The switched-mode converter is usually implemented by a buck converter with hysteresis current control. However, the slew rates of the load current and the inductor current of the buck converter can not match well when the slew rate of the load current has a wide variation range. The unmatched slew rates will lead to a high switching frequency of the buck converter or a large loss of the linear amplifier, which degrades the overall efficiency. In this paper, a multilevel converter is adopted to replace the buck converter in the parallel-form SLH ET power supply, and the hysteresis current control scheme is proposed for the multilevel converter to dynamically adjust its inductor current slew rate to approach that of the load current to improve the overall efficiency. The optimal design for the efficiency-related parameters including the inductor, the current hysteresis, and the number and values of the voltage levels in the multilevel converter is given. A prototype of the parallel-form SLH ET power supply with hysteresis current controlled multilevel converter is fabricated and tested in the lab. The measured overall efficiency is 79.4% when tracking the envelope of wideband code division multiple access (WCDMA) signal with 5 MHz bandwidth and outputs 18W average power, and a 3.8% efficiency improvement is achieved over that with the hysteresis current controlled buck converter.**

***Index Terms* — Power amplifier, envelope tracking, parallel-form, switch-linear hybrid, hysteresis current control, multilevel converter.**

I. Introduction

With the development of wireless communication, the data transmitted by the wireless communication systems have been increasing tremendously with the rapidly increased amount of users and the demand to multi-media services. In order to transmit more data within limited spectrum resources, spectrum-efficient modulation formats are employed [1]. As a consequence, the radio frequency (RF) signal features a variable envelope and a large peak-to-average power ratio (PAPR). For amplifying such RF signal without distortion, the linear power amplifiers (LPA) with good linearity, such as Class A and Class AB power amplifiers, are usually employed. However, the LPA fed by constant voltage is less efficient when amplifying a RF signal with a large PAPR. Envelope tracking (ET) technique [2], [3] could effectively boost the efficiency of the LPA by supplying the LPA with the voltage which is a duplicated and amplified version of the envelope signal. The schematic diagram of an ET system is shown in Fig. 1. The RF input signal passes through the delay unit and then amplified by the LPA. Meanwhile, the envelope of the RF input signal is extracted by the envelope detector and serves as the reference voltage of the ET power supply. The ET power supply amplifies the envelope signal linearly and supplies the LPA. The delay unit is used to compensate the delays introduced by the envelope detector and the ET power supply.

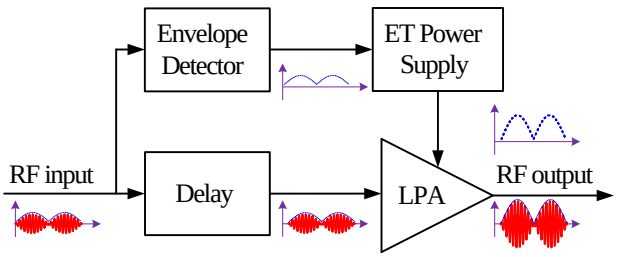

Fig. 1. Schematic diagram of an ET system.

The ET power supply is one of the key parts of the ET system for increasing the system efficiency [4]−[7]. Many topologies have been proposed for constituting the ET power supply, and among which, the switch-linear hybrid (SLH) ET power supply, consisting of a linear amplifier and one or multiple switched-mode converters, is the most popular structure due to its high efficiency and high linearity. The SLH ET power supply could be implemented in three forms, namely, series-form [8]−[10], parallel-form [11]−[13], and series-parallel-form [14], [15]. The series-parallel-form SLH ET power supply could achieve the highest efficiency but with complicated structure. The control strategy of the series-form SLH ET power supply is very simple and easy to implement. However, in order to achieve a relatively high efficiency, a multilevel converter is incorporated, and the number of voltage levels should be large, which increases the system complexity. Besides, the output voltage of the multilevel converter is a step-wave voltage, which contains abundant high frequency components. Too high frequency components will deteriorate the linearity of the system due to the limited bandwidth of the linear amplifier. Compared with the series-form and series-parallel-form ones, the parallel-form SLH ET power supply has less system complexity and can achieve better linearity. This paper focuses on the parallel-form SLH ET power supply, in which a voltage-controlled linear amplifier (VLA) and a current-controlled switched-mode converter (CSC) are connected in parallel. Since the VLA is less efficient, the current of the CSC is expected to track the load current accurately to minimize the current provided or sunk by the VLA to achieve a high efficiency.

Pulse width modulation (PWM) control [5] and hysteresis

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All the authors are with the Center for More-Electric-Aircraft Power System, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 211106, China (e-mail: yzwang@nuaa.edu.cn; ruanxb@nuaa.edu.cn; ly0719@nuaa.edu.cn; liying941128@nuaa.edu.cn).

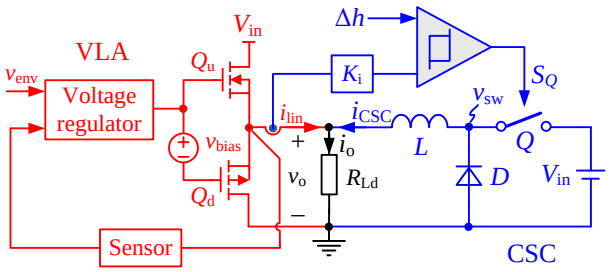


Fig. 2. Circuit of the parallel-form SLH ET power supply with HCC-2LC.

current control [16] can be used to control the current of CSC. Compared with the PWM control, the hysteresis current control has faster dynamic response and better robust, and has been widely used in the parallel-form SLH ET power supply. A buck converter is usually adopted to implement the CSC due to its simple structure [16], [17]. Basically, the buck converter is a two-level converter since two voltage levels, i.e., the input voltage and zero, are available, thus its inductor current only has a rising and falling slew rate to fit the load current. When adopting the hysteresis current control, the buck converter is defined as hysteresis current controlled two-level converter (HCC-2LC) hereinafter. As is known, the load current contains abundant components located in a wide frequency range, and the slew rate of the load current has a wide variation range. In order to achieve good tracking ability, the inductor in the HCC-2LC should be designed so small that its current slew rate is larger than the load current slew rate. However, when the output current slew rate is lower, the switching frequency of the HCC-2LC will be very high. This is due to the unmatched slew rates between the inductor current and load current. In this paper, a multilevel converter is adopted to replace the buck converter to enable a wider range of inductor current slew rate while maintain a low average switching frequency. Likewise, the multilevel converter adopting hysteresis current control is defined as the HCC-MLC. The inductor current slew rate of the HCC-MLC could be adjusted dynamically to match the load current slew rate by selecting appropriate voltage levels. Thus, the switching frequency of the HCC-MLC could be significantly reduced and the overall efficiency is improved.

In order to reduce the power loss of the linear amplifier in the parallel-form SLH ET power supply, the current hysteresis needs to be carefully considered. In the meanwhile, the HCC-MLC should have the ability of tracking the load current. Basically, the current tracking ability of the HCC-MLC is determined by the inductor and the voltage imposed on the inductor. So, this paper will present the optimized design method of the inductor, current hysteresis, and the number and values of the voltage levels in the HCC-MLC, in order to increase the overall efficiency of the parallel-form SLH ET power supply.

This paper is organized as follows. Section II reviews the operating principle of the parallel-form SLH ET power supply with HCC-2LC. Then, the parallel-form SLH ET power supply with HCC-MLC and the hysteresis current control scheme for the multilevel converter are proposed. Section III presents the optimized design method of the inductor, current hysteresis, and the number and values of the voltage levels in the HCC-MLC. In Section IV, a prototype is fabricated in the lab to track the envelope of wideband code division multiple access (WCDMA) signal

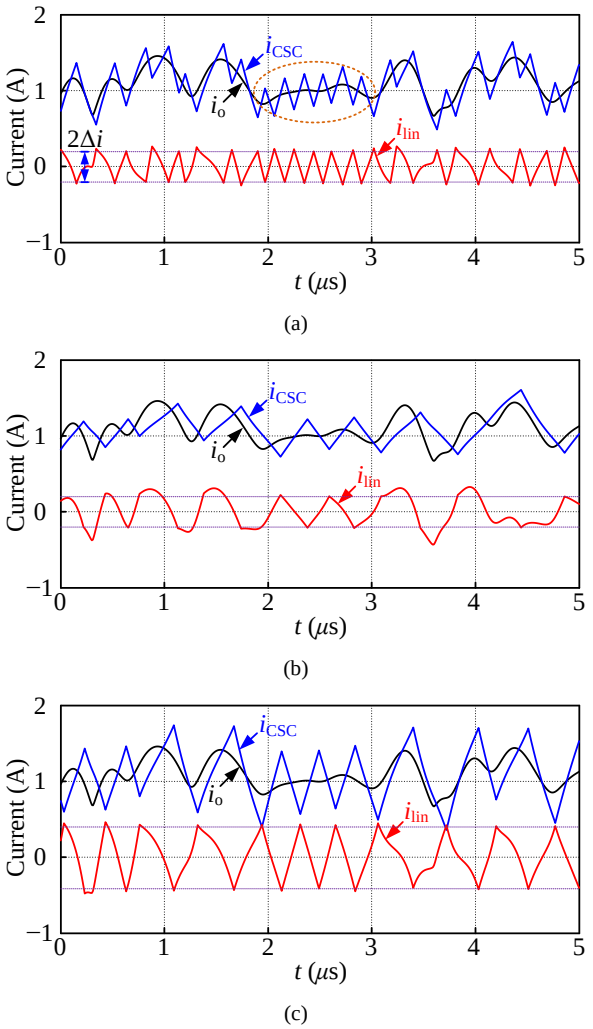


Fig. 3. Key waveforms of parallel-form SLH ET power supply with HCC-2LC at different L and Δi. (a) L = 3.2 μH and Δi = 0.2 A. (b) L = 8.0 μH and Δi = 0.2 A. (c) L = 3.2 μH and Δi = 0.4 A.

with 5 MHz bandwidth. The experimental results are provided to testify the proposed parallel-form SLH ET power supply with HCC-MLC. Finally, Section V concludes this paper.

II. Configuration and Operating Principle of the Parallel-Form SLH ET Power Supply

A. Parallel-Form SLH ET Power Supply With HCC-2LC

Fig. 2 shows the circuit of the parallel-form SLH ET power supply with HCC-2LC, where the VLA is implemented by a class AB linear amplifier and the CSC is implemented with a buck converter. The load of the ET power supply is an LPA, which can be approximately equivalent to a constant resistor and represented by R_{Ld} here. R_{Ld} can be measured by supplying the LPA with the load voltage v_o and sensing the load current i_o of the ET power supply at the demanded RF output power, and expressed as [18]

$$R_{Ld} = v_o / i_o \tag{1}$$

Note that for the convenience of measuring R_{Ld}, the ET power supply can be implemented with a simple VLA.

Referring to Fig. 2, the load voltage v_o is regulated by the VLA with closed-loop control. v_o is sensed and compared

with the envelope signal v_{env}, and the error is sent to the voltage regulator. The output of the voltage regulator drives Q_u and Q_d. v_{bias} is the bias voltage for avoiding the output voltage crossover distortion of the VLA. The hysteresis current control is adopted for the buck converter. The current of VLA, i_{lin}, is sensed with the sensor gain K_i, and then it is sent to the hysteresis comparator and compared with the hysteresis value Δh to produce the control signal of switch Q, S_Q. When $K_i i_{lin}$ is larger than Δh, $S_Q = 1$, and Q conducts; when $K_i i_{lin}$ is smaller than $-\Delta h$, $S_Q = 0$, and Q is turned off; otherwise, S_Q keeps unchanged.

Fig. 3 gives the key waveforms of the parallel-form SLH ET power supply with HCC-2LC when tracking the envelope of WCDMA signal with 5 MHz bandwidth at different L and Δi. Δi is the current hysteresis of i_{lin}, expressed as

$$\Delta i = \Delta h / K_i \tag{2}$$

Since the VLA suffers from low efficiency, the power processed by the VLA should be small for achieving a high overall efficiency. This requires the inductor current i_{CSC} should track i_o accurately and Δi needs to be small enough, as shown in Fig. 3(a). However, when the slew rate of i_o is relatively small, as shown in the dotted circle, the equivalent switching frequency of the CSC, f_s, is quite high. This is because the slew rate of i_{CSC} is relatively larger than the slew rate of i_o. Such a high switching frequency results in large switching loss and degrades the overall efficiency.

In order to decrease the f_s, a larger inductor can be used, and the corresponding current waveforms are shown in Fig. 3(b). As seen, i_{CSC} can not track i_o with large slew rate, and the current of the VLA, i_{lin}, will be outside the current hysteresis, leading to increased loss in VLA and degraded overall efficiency.

Fig. 3(c) shows the current waveforms with a larger current hysteresis. As seen, f_s can be decreased, but the loss of VLA is increased.

In conclusion, for the parallel-form SLH ET power supply with HCC-2LC, the slew rate of i_{CSC} should be large enough to track i_o. However, when the slew rate of i_o is lower, the large slew rate of i_{CSC} will lead to relatively high switching frequency and high switching loss. If the slew rate of i_{CSC} is not large enough to track i_o, the VLA will provide or sink large current, leading to larger loss. This is contradictory when designing the inductor due to the wide variation of the load current slew rate. So, it is better to dynamically adjust the slew rate of i_{CSC} for appropriately matching the load current slew rate.

B. Parallel-Form SLH ET Power Supply With HCC-2LC

Fig. 4 presents the circuit of the proposed parallel-form SLH ET power supply with HCC-MLC. Compared with Fig. 2, the buck converter is replaced by a multilevel converter. V_k (k = 1, 2, ..., m) is the discrete voltage level, and $0 = V_1 < V_2 < \ldots < V_m = V_{in}$, where m is the number of the voltage levels. SW_k (k = 2, 3, ..., m) is the selection switch, and S_k is the corresponding control signal. $S_k = 1$ represents switch SW_k conducts, and $S_k = 0$ represents switch SW_k is turned off. Since $V_1 = 0$, it is connected to the inductor naturally through the freewheeling diode D_1 when all the selection switches are shut down. For the convenience of illustration, S_1 is regarded as the selection signal of V_1 and it is always equal to 1. D_k (k = 2, 3, ..., m−1) is the block diode connected in series with SW_k to avoid short circuit of voltage levels with different amplitudes.

In order to control the inductor current i_{CSC} to track i_o, the current sensor is usually used to sense i_{lin} or i_{CSC}. However, the current sensor has a finite bandwidth, and it will introduce sampling error and delay to the current control loop and deteriorate the control performance. As an alternative, in high bandwidth applications, the current could be obtained with theoretical calculation to avoid using a current sensor [14], [15].

In the discrete time domain, the inductor current at the nth sampling instant, $i_{CSC}(n)$, can be calculated on the basis of i_{CSC} and the voltage across the inductor at the previous sampling instant, expressed as

$$i_{CSC}(n) = i_{CSC}(n-1) + \frac{\max(S_k \cdot V_k) - K_v \cdot v_{env}(n-1)}{L} T_{sp} \tag{3}$$

where, T_{sp} is the sampling period, K_v is the voltage amplification factor of the ET power supply, and max ($S_k \cdot V_k$) is the maximum of $S_k \cdot V_k$ (k = 1, 2, ..., m). For example, when m = 4, $S_1 = S_2 = S_3 = 1$, and $S_4 = 0$, v_{sw} equals to max ($S_k \cdot V_k$) = $S_3 \cdot V_3 = V_3$. The calculated $i_{CSC}(n)$ according to (3) is sent to hysteresis current control scheme for the multilevel converter to generate $S_k(n)$ (k = 2, 3, ..., m), which are used to control the switches and calculate the inductor current at the next sampling instant, $i_{CSC}(n+1)$. It is worthy to note that the current calculation error is inevitable, and the accumulated error may cause i_{CSC} out of control. To eliminate the calculation error, i_{CSC} is reset by shutting down all the selection switchers in the multilevel converter for a

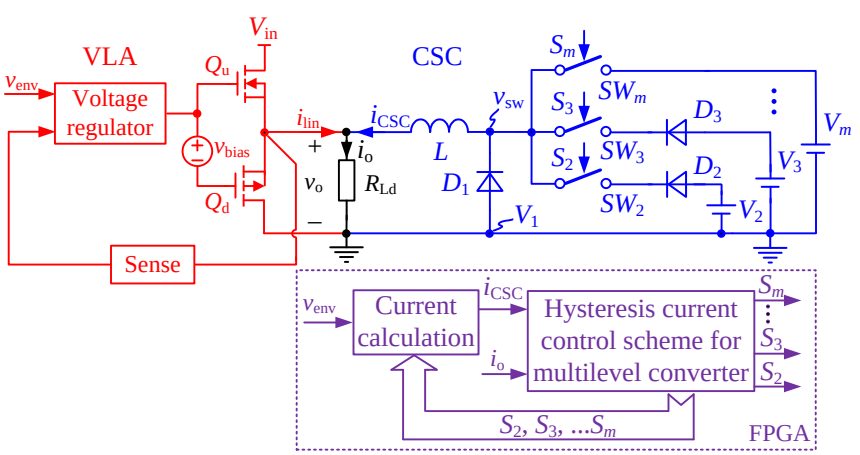


Fig. 4. Circuit of the parallel-form SLH ET power supply with HCC-MLC.

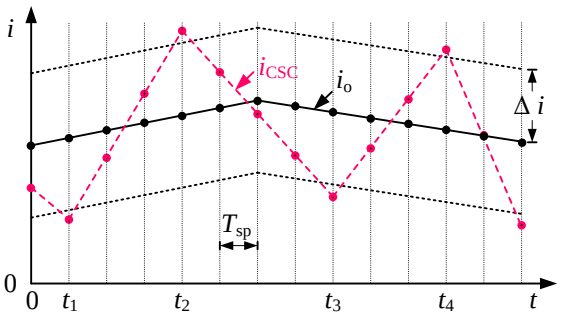


Fig. 5. Key current waveforms of the hysteresis current control for the multilevel converter.

short time every several hundreds of switching periods, and T_{con} = 327 μs and T_{reset} = 0.68 μs are selected in this paper, where T_{con} and T_{reset} are the operation and reset time of CSC. The selection of T_{reset} should guarantee the i_{CSC} can be decreased to zero. Besides, T_{reset} should be as small as possible since the load current is mainly provided by the VLA during the reset time, and a large T_{reset} will decrease the system efficiency. Since the selected T_{reset} is much smaller than T_{con}, the decreased efficiency can be neglected.

The main idea of the hysteresis current control for multilevel converter is to select appropriate voltage level to adjust the slew rate of i_{CSC} to match the slew rate of i_o and thus decrease f_s. Fig. 5 shows the key current waveforms of the hysteresis current control for the multilevel converter, where three possible cases will occur, which are discussed as below.

Case I: if $i_{CSC}(n) \le i_o(n) - \Delta i$, such as the situations at t_1 and t_3 in Fig. 5, i_{CSC} should be increased to track i_o. According to the slew rate of i_o, which may be positive or negative, there are two possible sub-cases.

Case I-A: if $i_o(n+1) \ge i_o(n)$, such as the situation at t_1, the rising rate of i_{CSC} is required to be larger than that of i_o to guarantee the tracking ability, and v_{sw} should meet

$$v_{sw}(n) > v_o(n) + L \cdot \frac{i_o(n+1) - i_o(n)}{T_{sp}} \tag{4}$$

In order to decrease f_s as much as possible, the slew rate of i_{CSC} should be close to that of i_o. So, the minimal voltage level satisfying (4) is selected.

Case I-B: if $i_o(n+1) < i_o(n)$, such as the situation at t_3, the second term at the right side in (4) is smaller than zero. At this time, v_{sw} is required to meet

$$v_{sw}(n) > v_o(n) \tag{5}$$

And the minimal voltage level satisfying (5) is selected to minimize f_s.

Case II: if $i_{CSC}(n) \ge i_o(n) + \Delta i$, such as the situations at t_2 and t_4 in Fig. 5, v_{sw} should be lower than v_o to force i_{CSC} to decrease. Likewise, according to the polarity of the slew rate of i_o, there are two possible sub-cases.

Case II-A: if $i_o(n+1) < i_o(n)$, such as the situation at t_4, the decaying rate of i_{CSC} should be larger than that of i_o, and v_{sw} is required to meet

$$v_{sw}(n) < v_o(n) + L \cdot \frac{i_o(n+1) - i_o(n)}{T_{sp}} \tag{6}$$

And the maximal voltage level satisfying (6) is selected.

Case II-B: if $i_o(n+1) \ge i_o(n)$, such as the situation at t_2, the second term at the right side of (6) is larger than zero. At this time, v_{sw} is required to be smaller than v_o to make i_{CSC} decrease, i.e.,

$$v_{sw}(n) < v_o(n) \tag{7}$$

And the maximal voltage level satisfying (7) is chosen.

Case III: if $i_o(n) - \Delta i < i_{CSC}(n) < i_o(n) + \Delta i$, v_{sw} keeps unchanged.

In conclusion, v_{sw} can be expressed as

$$v_{sw}(n) = \begin{cases} \min[V_1, V_2, ..., V_m] > v_o(n) + L \cdot \dfrac{i_o(n+1) - i_o(n)}{T_{sp}} & \text{Case I-A} \\ \min[V_1, V_2, ..., V_m] > v_o(n) & \text{Case I-B} \\ \max[V_1, V_2, ..., V_m] < v_o(n) + L \cdot \dfrac{i_o(n+1) - i_o(n)}{T_{sp}} & \text{Case II-A} \\ \max[V_1, V_2, ..., V_m] < v_o(n) & \text{Case II-B} \\ v_{sw}(n-1) & \text{Case III} \end{cases} \tag{8}$$

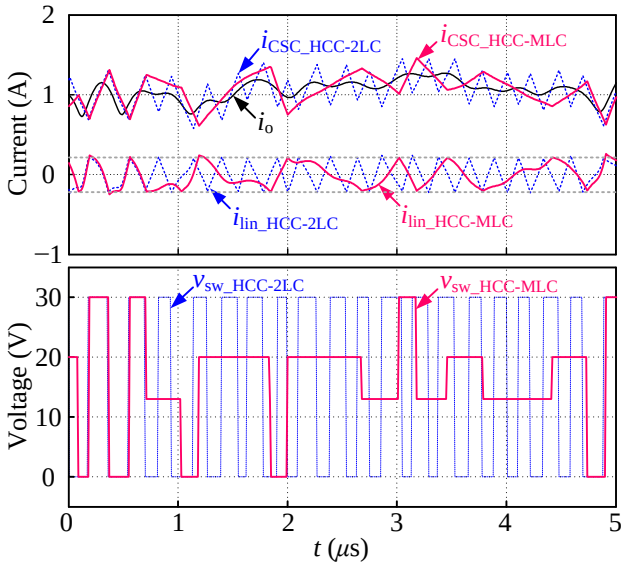


Fig. 6. Simulated waveforms of the parallel-form SLH ET power supplies with HCC-2LC and HCC-MLC, respectively.

Fig. 6 shows the simulated waveforms of the parallel-form SLH ET power supplies with HCC-2LC and HCC-MLC, respectively, when tracking the envelope of WCDMA signal with 5 MHz bandwidth. Here, L = 4 μH and Δi = 0.2 A. The multilevel converter is designed to have four voltage levels, and the values of the voltage levels are 0 V, 13 V, 20 V, and 30 V. The selection of the number and values of the voltage levels will be discussed in Section III. From Fig. 6, it is clear to see that: 1) the HCC-MLC can adjust its current slew rate by selecting appropriate voltage levels, and thus f_s can be greatly decreased; and 2) i_{lin} is well controlled within $\pm\Delta i$, and the loss of VLA is nearly the same as that with HCC-2LC.

III. Optimized Parameters Design

The inductor L has a large impact on the current tracking ability of the CSC and the loss of VLA. Δi decides the amplitude of i_{lin}, which impacts the loss of VLA directly. Moreover, Δi also affects f_s, and f_s is also related with the

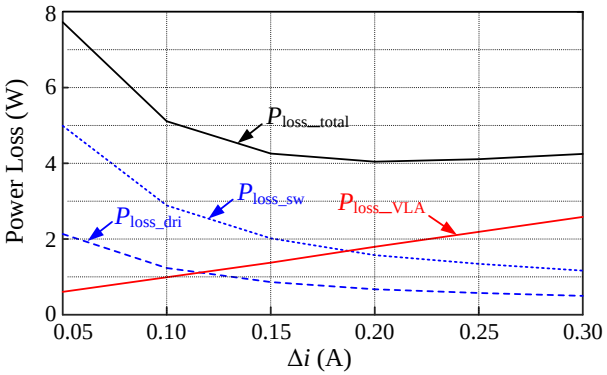


Fig. 7. Curves of the losses versus Δi when L = 4 μH.

voltage levels in the HCC-MLC. Thus, these parameters need to be optimally designed for achieving a high overall efficiency.

A. Design of the Inductor and Current Hysteresis

In order to ensure the inductor current, i_{CSC}, tracks the load current i_o accurately, the inductor current slew rate should be equal to or larger than the slew rate of the load current at all time [19]. However, the designed inductor will be very small, resulting in a high switching loss. To trade off the switching loss of the CSC and the loss of the VLA, the average slew rate of the load current, SRi_o, is selected to design the inductor [16], expressed as

$$SRi_o = \frac{1}{N_p}\sum_{n=1}^{N_p-1}\frac{\left|i_o(n+1)-i_o(n)\right|}{T_{sp}} \tag{9}$$

where, N_p is the length of the envelope signal, and it is expected to be large enough to get the accurate SRi_o of the envelope.

The rising and falling rate of the i_{CSC} at each instant should be larger than SRi_o to guarantee the tracking ability to i_o, and the inductor L should meet the requirement, i.e.,

$$L < \begin{cases} \dfrac{V_{in}-v_o(n)}{SRi_o} & \text{when } i_o(n+1) > i_o(n) \\ \dfrac{v_o(n)}{SRi_o} & \text{when } i_o(n+1) < i_o(n) \end{cases} \tag{10}$$

From (10), L < 4.34 μH is obtained with the specifications given in Table II in Section IV. Finally, L = 4 μH is selected.

As mentioned before, Δi affects i_{lin} and f_s. So, when designing Δi, the loss of VLA P_{loss_VLA}, the switching loss P_{loss_sw}, and the driver loss P_{loss_dri} of the CSC should be considered. Δi is intentionally designed to be quite smaller than the dc component of i_{CSC} for reducing the power loss in VLA. Thus, the variation of Δi has small effect on the root-mean-square of i_{CSC}, and the loss of inductor and the switch conduction loss are assumed to be unchanged for simplifying the design process.

Here, a class AB linear amplifier is used to realize VLA, and its instantaneous loss p_{loss_VLA} can be expressed as

$$p_{loss\_VLA} = \begin{cases} (V_{in}-v_o)\cdot i_{lin} & \text{when } i_{lin} > 0 \\ v_o \cdot i_{lin} & \text{when } i_{lin} < 0 \end{cases} \tag{11}$$

P_{loss_VLA} can be calculated by averaging (11). P_{loss_sw}, P_{loss_dri}, and the sum of these losses, P_{loss_total}, can be expressed as

TABLE I

OPTIMIZED VALUES OF VOLTAGE LEVELS AND f_s AT DIFFERENT m

m	Values of Voltage Levels (V)	f_s (MHz)
2	0, 30	3.11
3	0, 14, 30	2.44
4	0, 13, 20, 30	2.28
5	0, 12, 20, 22, 30	2.34

$$P_{loss\_sw} \approx \frac{1}{2}\cdot V_{in}\cdot\frac{K_v\cdot v_{env\_avg}}{R_{Ld}}\cdot\left(t_{on}+t_{off}\right)\cdot f_s \tag{12}$$

$$P_{loss\_dri} = V_{dri}\cdot Q_g\cdot f_s \tag{13}$$

$$P_{loss\_total} = P_{loss\_VLA} + P_{loss\_sw} + P_{loss\_dri} \tag{14}$$

where, v_{env_avg} is the average value of v_{env}, which can be obtained by using the probability density function of v_{env} [8]; t_{on} and t_{off} are the turn-on and turn-off times of the selection switches; f_s is the equivalent switching frequency of the CSC, which can be calculated by counting the turn-on times of all selection switches during $N_p \cdot T_{sp}$; and V_{dri} and Q_g are the driving voltage and the total gate charge of the selection switch, respectively.

Fig. 7 shows the curves of the power losses versus Δi when L = 4 μH. As seen, with the increase of Δi, P_{loss_VLA} increases, P_{loss_dri} and P_{loss_sw} decrease, and P_{loss_total} decreases first and then increases. P_{loss_total} gets its minimum value when Δi = 0.2 A. Thus, Δi = 0.2 A is selected.

B. Design of the Number and Values of the Voltage Levels in the HCC-MLC

As seen from Fig. 6, the losses of VLA are nearly the same when the parallel-form SLH ET power supplies are implemented with HCC-2LC and HCC-MLC. Thus, the optimization goal of the HCC-MLC can be equivalent to achieving a lowest f_s to reduce its loss. Table I shows the optimized values of the voltage levels and the corresponding f_s at different number of voltage levels, m [8]. As seen, the adoption of HCC-MLC (m > 2) could effectively decrease f_s compared with the HCC-2LC (m = 2). Besides, f_s decreases first and then increases with the increase of m, and f_s is minimized when m = 4. Since f_s when m = 4 is slightly lower than that when m = 3. Here, m = 3 is selected for reducing the system complexity, and the optimized values are 0 V, 14 V, and 30 V.

IV. EXPERIMENTAL VERIFICATIONS

A. ET Power Supply Tests

In order to verify the effectiveness of the proposed parallel-form SLH ET power supply with HCC-MLC and the hysteresis current control for the multilevel converter, a prototype is fabricated in the lab, as shown Fig. 8. The specifications are given in Table II, and the devices and controllers used in the prototype are listed in Table III.

Fig. 9 gives the circuit of the multi-level converter (m=3).

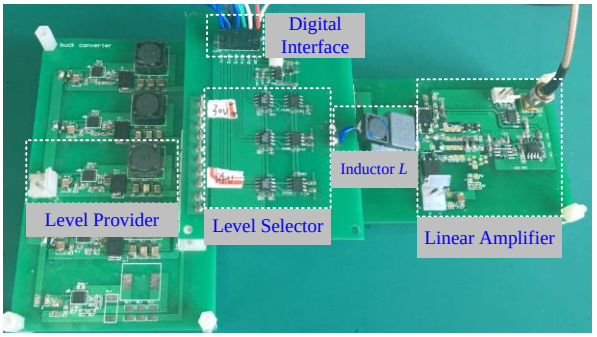


Fig. 8. Photograph of the proposed ET power supply with HCC-MLC.

TABLE II

SPECIFICATIONS OF THE PROPOSED ET POWER SUPPLY WITH HCC-MLC

Specifications	Value
Signal bandwidth	5 MHz
System input voltage V_{in}	30 V
Output voltage range v_o	9.6 V ~ 26.4 V
Average output power	18 W
PAPR	3.5 dB

TABLE III

DEVICES AND CONTROLLERS IN THE PROTOTYPE

Level Provider	
Integrated Power module	TPS54541 (TI) ×1
Freewheeling diode	SK56 (MCC) ×1
Filter inductor	100 μH ×1 (Würth Elektronik)
Filter capacitor	47 μF (Murata) ×3
Level Selector	
Selection switches	IRLR024 (Vishay)×2
Block diode D_2	SK56 (MCC) ×1
Freewheeling diode D_1	SK56 (MCC) ×1
Driver ICs	IL711 (NVE) × 1
Isolator ICs	ISL89410 (Intersil) ×1
Inductor L	4 μH (Würth Elektronik)
Linear Amplifier	
Linear regulating devices	IRLR024 (Vishay) ×1 FDD5614P(Vishay) ×1
Operational amplifiers	THS4012 (TI) ×1 THS3001 (TI) ×1
Digital Control Platform	
FPGA	XC3S500E (XILINX) ×1
T_{sp}	10 ns

Compared with the buck converter, a level selector consisting of switch Q_2 and block diode D_2 and a level provider implemented by a buck converter are added, as

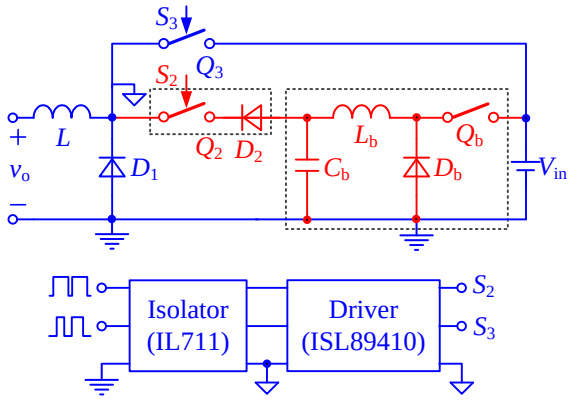


Fig. 9. Circuit of the multilevel converter when m = 3.

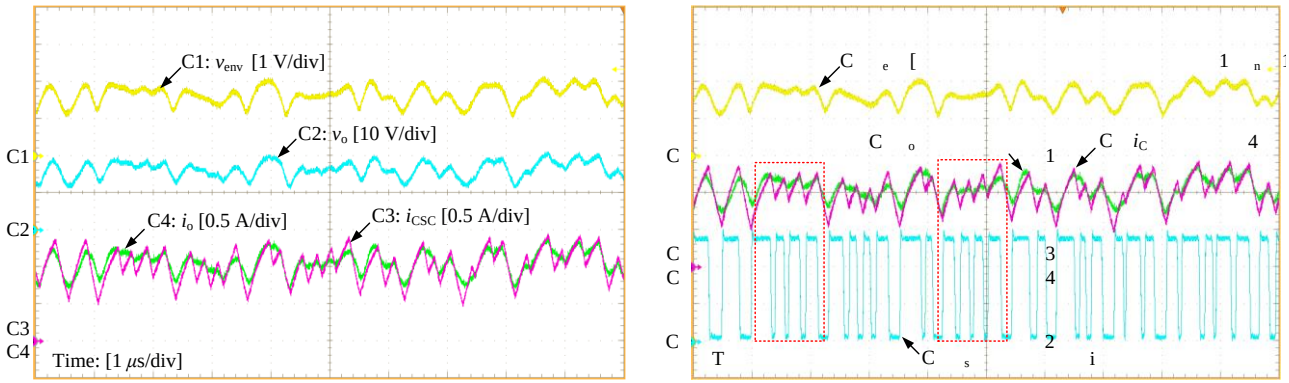
shown in the dotted blocks. IL711 and ISL89410 are dual channel isolator and driver, respectively, and they are used for controlling Q_2 and Q_3. This means that the level selector does not need additional isolator and driver. Besides, the added buck converter for constituting the level provider can be easily implemented with the integrated power module TPS54541 from TI, which integrates switch Q_b and its controller and driver. Thus, the increased system complexity is limited.

As seen from Fig. 9, there are two inductors in the system. One is the inductor L, which is 4 μH, and the other one is the filter inductor L_b of the buck converter in the level provider, and its inductance is 100 μH. The high frequency load current flows through the inductor L, thus this inductor should have a low dc resistance to decrease its loss and high self resonant frequency to guarantee its inductance when operating at several megahertz. While for L_b, the requirement for self resonant frequency can be lowered, since the dynamic response of the buck converter does not need to be fast and the high frequency load current is mainly provided by the filter capacitor C_b.

The digital control platform of the system is implemented with a field programmable gate array (FPGA). In order to guarantee the current control accuracy of the CSC, the sampling frequency of the FPGA should be much larger than the switching frequency of the CSC, and 100 MHz is selected here, which means the T_{sp} is 10 ns.

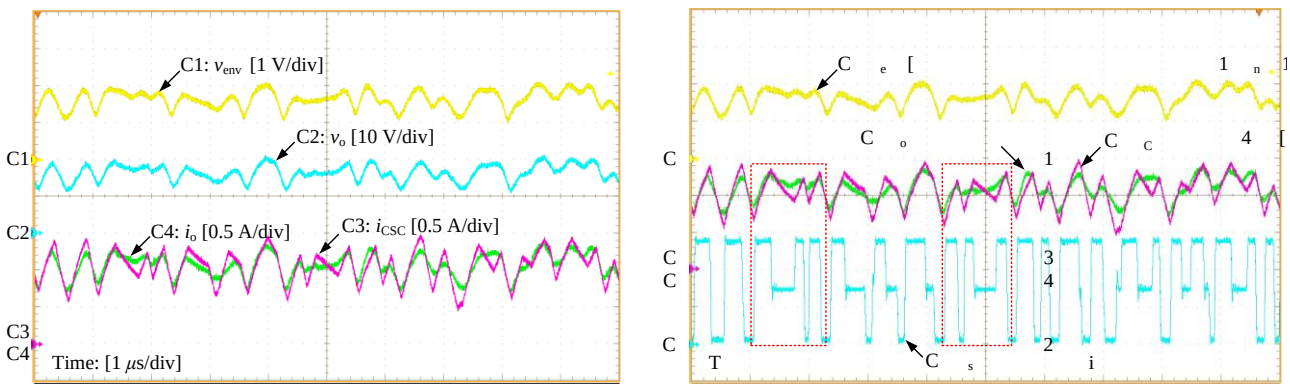
Figs. 10 and 11 show the experimental waveforms of the parallel-form SLH ET power supplies with HCC-2LC and HCC-MLC, respectively, where v_{env} is the envelope signal, v_o is the load voltage, i_o is the load current, i_{CSC} is the current of CSC, and v_{sw} is the step-wave voltage. As seen from Fig. 10(a) and Fig. 11(a), v_o tracks v_{env} accurately, and i_{CSC} is well controlled to follow i_o. As seen from Fig. 10(b), the switching frequency f_s is very high when tracking i_o with small slew rate, as shown in the dotted circles. This is because that only two voltage levels, i.e., V_{in} and zero, are available in the buck converter, and the inductor current slew rate can not match the slew rate of i_o in a wide variation range. On the contrary, more voltage levels are available in the multi-level converter, and the appropriate voltage levels could be selected to adjust the slew rate of i_{CSC} to match the slew rate of i_o, and thus f_s can be reduced, as shown in the dotted circles in Fig. 11(b).

Table IV shows the loss distribution, efficiency, and linearity of the parallel-form SLH ET power supplies with HCC-2LC and HCC-MLC, respectively, where P_{out} is the output power of the ET power supply; P_{loss_VLA} is the loss of



(a) (b)

Fig. 10. Experimental waveforms of the parallel-form SLH ET power supply with HCC-2LC. (a) v_{env}, v_o, i_o and i_{CSC}. (b) v_{env}, i_o, i_{CSC}, and v_{sw}.



(a) (b)

Fig. 11. Experimental waveforms of the parallel-form SLH ET power supply with HCC-MLC. (a) v_{env}, v_o, i_o, and i_{CSC}. (b) v_{env}, i_o, i_{CSC}, and v_{sw}.

TABLE IV

LOSS DISTRIBUTION, EFFICIENCY, AND LINEARITY OF THE PARALLEL-FORM SLH ET POWER SUPPLIES

	With HCC-2LC	With HCC-MLC
P_{out} (W)	17.51	17.79
P_{loss_VLA} (W)	1.55	1.61
P_{loss_CSC} (W)	3.51	2.42
P_{loss_static} (W)	0.6	0.6
η_{ET} (%)	75.6	79.4
NMSE (%)	0.23	0.26

TABLE V

COMPARISON WITH PREVIOUS WORKS USING MULTILEVEL CONVERTER

	[5]	[12]	This work
Output voltage range (V)	10 ~ 26	5 ~ 28	9.6 ~ 26.4
Average output power (W)	25	10.4 / 3.2	~20
PAPR (dB)	2.8	~3 / ~8	3.5
Signal	Sine	EDGE/WCDMA	WCDMA
Bandwidth (MHz)	1	0.4 / 5	5
Efficiency (%)	72.4	74.7 / 49.9	79.4

VLA; P_{loss_CSC} is the loss of CSC, including the loss of the level provider, level selector, and inductor L; P_{loss_static} is the static loss, including the loss of FPGA and other ICs; and η_{ET} is the overall efficiency of the ET power supply. The linearity of the ET power supply is evaluated with the normalized mean square error (NMSE) [8]. As seen, with the HCC-MLC, P_{loss_CSC} is effectively reduced without increasing P_{loss_VLA} compared with HCC-2LC, and a 3.8% efficiency improvement can be achieved. Besides, the NMSEs of the two ET power supplies are nearly the same and they are very small due to the adoption of the VLA, indicating that the ET power supplies have good linearity.

Table V shows the comparison of the proposed ET power supply with previous works using multilevel converter. The step-wave approach proposed in [5] adopts a PWM control method, and the switching frequency of each selection switch is equal to the bandwidth of the envelope signal f_{BW}, thus the equivalent f_s of the multilevel converter is k times of f_{BW}, where k is the number of selection switches. In order to achieve the desired tracking performance, k is required to be relatively large and k = 5 is chosen in [5]. In [12], the multilevel converter is also PWM controlled, which could reduce the filter when compared with the two-level converter. However, the equivalent f_s still needs to be larger than 10 f_{BW} to ensure the tracking accuracy. Benefited from the fast dynamic response of the hysteresis current control, the equivalent f_s needed in the proposed ET power can be reduced compared with the PWM control. Besides, the adoption of HCC-MLC could decrease the equivalent f_s further. Thus, the parallel-form SLH ET power supply with HCC-MLC presented in this paper is expected to achieve a higher overall efficiency in high bandwidth applications. As seen from Table IV, the proposed topology still could

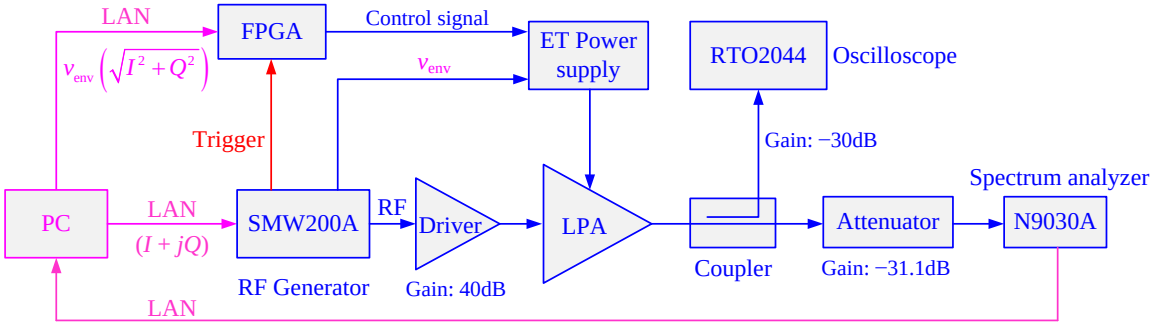


Fig. 12. ET system configuration.

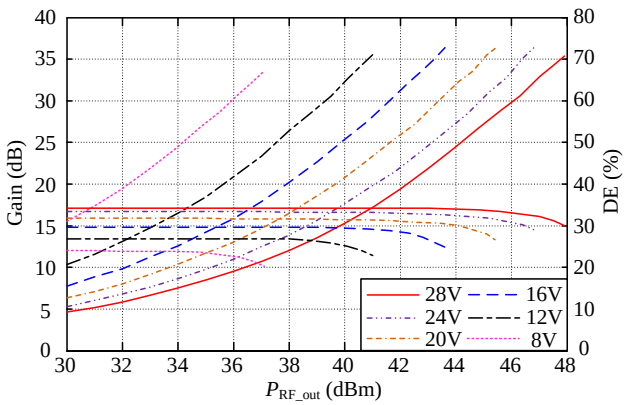


Fig. 13. Gain and DE curves of the LPA versus RF output power under different supply voltages.

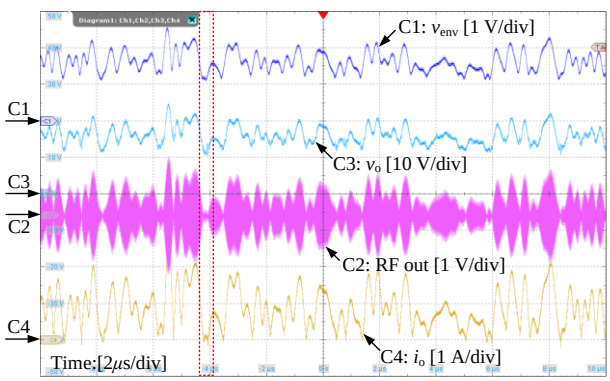


Fig. 14. Waveforms of the ET system.

achieve a higher overall efficiency when tracking an envelope signal with a wider bandwidth under the similar conditions of output voltage range, average output power, and PAPR.

B. ET System Tests

Fig. 12 shows the ET system established for verifying the effectiveness of the proposed ET power supply when its load is a real LPA and estimating the performance of LPA. The baseband signal $S_{BB} = I + jQ$ and its digital envelope signal $v_{env} = \sqrt{I^2+Q^2}$ are sent to the SMW200A vector signal generator and FPGA from a PC directly. The RF signal and its corresponding analog envelope signal are generated by the SMW200A, and the RF signal is delayed for a period of time to synchronize the input RF signal and the supply voltage of the LPA. The control signal of the ET power supply is generated by the FPGA, which is triggered by the

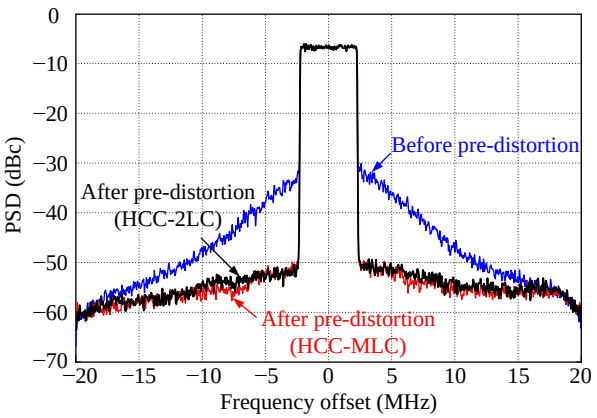


Fig. 15. Measured WCDMA spectrum before and after DPD is adopted.

SMW200A to synchronize the envelope signal and the control signal. The LPA works at class AB and operates at 1.6 GHz.

Fig. 13 shows the measured gain and drain efficiency (DE) curves of the LPA versus RF output power P_{RF_out} under different supply voltages, which could cooperate with the power generation distribution (PGD) of the output RF signal to estimate the DE of the LPA when amplifying a RF signal with variable envelope.

Fig. 14 gives the waveforms of the above ET system when transmitting a WCDMA signal with a 8.5 dB PAPR. As shown, the output voltage of the parallel-form SLH ET power supply, v_o, follows the envelope signal v_{env} precisely, and v_o and the RF signal are synchronized. Besides, the waveform of v_o and i_o is very similar, and the RF PA can be treated as a resistor. In high power levels, this resistor is almost keeps constant. While in low power levels, since the RF input power is very small, the i_o is very small, as the dotted block shows. However, the v_o is still very high to avoid gain collapse. Thus, the equivalent resistor increases. And the R_{Ld} mentioned in (1) is chosen at high power levels.

When delivering 39.5 dBm output power, the measured drain efficiencies of the LPA are 49.7% and 32.0% when the LPA is powered by the proposed ET power supply and a constant voltage of 28V, respectively. Obviously, the proposed ET power supply could effectively boost the efficiency of the LPA, and a 18% efficiency improvement is achieved. The linearity of the LPA is evaluated with the adjacent channel power ratio (ACPR). The measured output spectrum is shown in Fig. 15. As seen, the ACPR of the LPA is −28.9 dBc without the digital pre-distortion (DPD), and it is reduced to −45.4 dBc when the DPD is adopted [20]. Meanwhile, the performance of the LPA is also tested when the ET power supply with HCC-2LC is adopted. The drain

efficiency reaches 49.4%, and the ACPR with DPD is −45.2 dBc, as shown in Fig. 15. The results are very similar to that of the ET power supply with HCC-MLC, which is in accordance with expectation since the performance of the LPA is mainly decided by its supply voltage, i.e., the output voltage of the ET power supply, and the output voltages of the two ET power supplies are almost the same since they track the same reference voltage v_{env} and have similar linearity, as shown in Table IV. Besides, the measured efficiency of the overall ET system with the proposed ET power supply is 38.7%, which is 2% higher than that with the HCC-2LC.

From the above illustration, it can be concluded that the efficiency of the LPA can be significantly improved when adopting the proposed ET power supply, and its linearity can be enhanced to satisfy the spectral masks by using DPD.

VI. Conclusions

The operating principle of the parallel-form SLH ET power supply with HCC-2LC is analyzed in this paper, and it is pointed out that the slew rates of the load current and the inductor current can not match well when the slew rate of the load current has a wide variation range, which will result in a high switching frequency of CSC or a large loss of VLA, and thus degrade the overall efficiency. A parallel-form SLH ET power supply with HCC-MLC is presented in this paper, and the hysteresis current control scheme for the multilevel converter is proposed, which could adjust the slew rate of the inductor current by selecting appropriate voltage levels to approximate that of the load current. As a consequence, the switching frequency of CSC is reduced without increasing the loss of VLA, and thus the overall efficiency is improved. The optimized design of the efficiency-related parameters including the inductor, the current hysteresis, and the voltage levels in the HCC-MLC are given. Prototypes with HCC-MLC and HCC-2LC, respectively, are fabricated and tested. The experimental results verify the effectiveness of the proposed topology and control strategy. The overall efficiency is measured as 79.4% when tracking the WCDMA envelope signal with 5 MHz bandwidth and a 3.8% efficiency improvement is achieved over that with HCC-2LC. Finally, an ET system is established for transmitting the WCDMA signal with a 8.45 dB PAPR to further verify the proposed ET power supply, and the measured DE of the LPA reaches 49.7% when the LPA outputs 39.5 dBm average power, a 18% efficiency improvement over that of LPA supplied by 28 V constant voltage, and the ACPR of the LPA can be decreased to −45.4 dBc by adopting DPD.

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Yazhou Wang received the B. S. degrees in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2013, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include envelope tracking power supplies and dc-dc converters.

Xinbo Ruan (M'97-SM'02-F'16) received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

In 1996, he joined the Faculty of Electrical Engineering Teaching and Research Division, NUAA, where he became a Professor in the College of Automation Engineering in 2002 and has been engaged in teaching and research in the field of power electronics. From August to October 2007, he was a Research Fellow in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong, China. Since March 2008 to Sep. 2011, he was also with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, China. He is a Guest Professor with Beijing Jiaotong University, Beijing, China, Hefei University of Technology, Hefei, China, and Wuhan University, Wuhan, China. He is the author or co-author of 9 books and more than 200 technical papers published in journals and conferences. His main research interests include soft-switching dc-dc converters, soft-switching inverters, power factor correction converters, modeling the converters, power electronics system integration and renewable energy generation system.

Prof. Ruan was a recipient of the Delta Scholarship by the Delta Environment and Education Fund in 2003 and was a recipient of the Special Appointed Professor of the Chang Jiang Scholars Program by the Ministry of Education, China, in 2007. From 2005 to 2013, and since 2017 again, he served as Vice President of the China Power Supply Society (CPSS). Since 2008, he has been a member of the Technical Committee on Renewable Energy Systems within the IEEE Industrial Electronics Society. Currently, he serves as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS ON POWER ELECTRONICS, AND the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS - II. He is an IEEE Fellow.

Yang Leng received the B.S. and M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2015 and 2018, respectively.

His main research interests include digital control and dc-dc converters.

Ying Li received the B.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2017, where she is currently pursuing the M.S. degree in electrical engineering.

Her main research interests include digital control, and dc-dc converters.